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CMOS instrumentation amplifier designing concept for low power sensor applications

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Abstract

The present paper presents a high performance instrumentation amplifier based on operational amplifier (op-amp) for low power applications. This instrumentation amplifier (IA) is designed for low power while maintaining the high PSRR, high CMRR as well as other design constraints. The Most effective topology current feedback is illustrated in this article using some dynamic techniques for offset & noise compensation. Current feedback chopper stabilization technique has been widely used in amplifiers which are based upon the principles of modulation and demodulation. Thus, the functionality and overall performance of MODEM circuits determines the realization and attainment of chopper stabilization for flicker (1/f) noise and offsets reduction purposes. A different technology variation 800nm to 180nm has been introduced in this review to design precise instrumentation amplifier.

Keywords: instrumentation amplifier, low power sensor applications, dynamic techniques.

1. Introduction

The trends of technological development are heavily focused on improving and expanding the integration of digital processing in everyday life. This development demands that analog circuitry keep up with the phase. CMOS instrumentation amplifiers (IAs) have grown extensively for emerging sensor circuit applications such as integrated strain sensors, hall sensors, thermocouples, micro-electromechanical system sensor arrays, multichannel sensing systems and integrated biosensors [1-2]. Sensors are used to translate information from various physical domains like thermal, mechanical, and magnetic to information measurable in electrical domain. This electrical signal is generally an analog signal and needs to be translated to digital signal for further signal processing. The system involved in the chain of converting the analog signal from sensors, to digital signal is called sensor readout system. In all these applications, low power consumption is desired as it results in lower system costs and in the case of battery powered systems, longer operating lifetime.

Instrumentation amplifier forms an important part of the low power applications since it needs to distinguish noise and the desired signal which is of small amplitude [3]. The Processing circuitry consists of an instrumentation amplifier which is used for precision amplification of differential DC/AC signals while rejecting large values of common mode signal. Instrumentation amplifiers that operate on +/- 5V are commonly used to take advantage over large voltage range [4]. A low noise and low power consumption instrumentation amplifier is the key design for detecting the small level signals in the low power applications. However, in current VLSI technology the flicker noise becomes a significant issue which limits the minimum observable signal in amplifier circuit at low frequency [5-6]. The Well-known design used in a low power sensor system, is an operational amplifier, must manifest very low input referred noise, low power consumption and high Common Mode Rejection Ratio (CMRR). In this paper, a low voltage, low noise and high CMRR operational amplifier for portable monitoring system is proposed. The operational amplifier is able to work under 1-V supply, has high CMRR and low noise. Devices may pertain to different inversion region like weak, moderate and strong. Out of these three regions, MOSFET operating in saturation region is most suitable for low power applications where devices are operated either at low voltage/current or both.

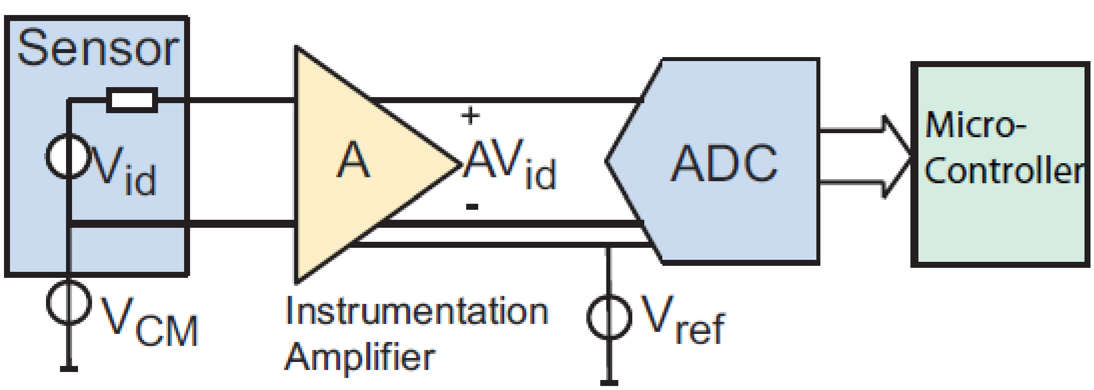

Fig 1: Block diagram of typical sensor readout system

Figure 1 shows a typical sensor readout system whose output assumed to be in voltage. The differential voltage (Vid) from the readout system is amplified by the amplifier (A) and given to an Analog to Digital Converter (ADC). ADC converts the information to digital domain. This digital data can be processed by a micro-controller. As typical sensor signals are very small (in µV), an amplifier A is used to increase the signal before passing it to ADC. The main functions of Instrumentation Amplifier in this system are to

- Amplify the differential voltage (Vid).
- Reject the sensor common mode voltage (VCM).
- Level shift to ADC reference voltage (Vref).

As these amplifiers are used to detect very small input differential signals, the input referred errors (due to offset & noise) of such amplifiers should be well below the minimum input signal. In recent years, current feedback topology has become very popular [7-9]. However, like all amplifiers, a CFIA will suffer from offset, which, in a CMOS implementation, can be in the order of several mV. This is too high for precision applications, and so dynamic techniques such as chopping and auto-zeroing have been used to achieve micro-volt offset levels [10-13].

A brief review of different topology used to design instrumentation amplifier is provided in section II. In section III, most emerging topology current feedback instrumentation amplifier has been given and formulation of method has been provided. Noise minimization has been also presented. Section IV explains the state-of-art of previous work to design by minimizing the offset voltage. Section V, gives the conclusion.

2. Instrumentation Amplifier Design Topology

Instrumentation amplifier can be designed from an op-amp circuit but the behavior of instrumentation amplifier is intensely different than an op-amp and difficult to design precisely from single op-amp circuit. Instrumentation amplifier can be designed by several different ways. The commonly used techniques are difference amplifier, two op-amps, and three op-amps, switched capacitor, capacitively coupled, current mode, resistive feedback and current feedback instrumentation amplifier.

The classical three op-amp instrumentation amplifier shown in figure 2 having inputs V_{IN-} & V_{IN+} defined by the input polarity of difference amplifier A_3. These inputs can be categories as common mode voltage and difference voltage. These voltages cab be expressed as:

$$V_{CM} = (V_{IN-} + V_{IN+})/2 \text{ and } V_D = V_{IN+} - V_{IN-} \qquad (1)$$

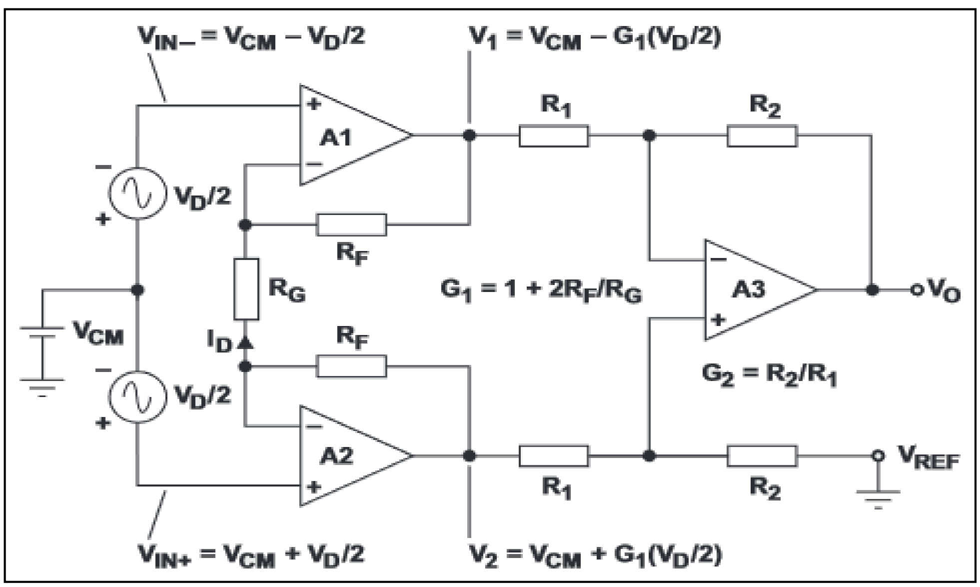

Fig 2: Three Op-amp Instrumentation Amplifier [14]

Now input voltages can be calculated in terms of common mode and difference voltage as:

$$V_{IN+} = V_{CM} + V_D/2 \text{ and } V_{IN-} = V_{CM} - V_D/2 \qquad (2)$$

Difference voltage V_D is applied across gain resistor as shown in figure 4 to calculate current, I_D

$$I_D = (V_{IN-} + V_{IN+})/R_G = V_D/R_G \qquad (3)$$

The output voltage of first stage op-amps are

$$V_1 = V_{CM} - \frac{V_D}{2} - I_D.R_F$$

and

$$V_2 = V_{CM} + \frac{V_D}{2} + I_D.R_F \qquad (4)$$

Replacing the current value from equation 3 into equation 4

$$V_1 = V_{CM} - \frac{V_D}{2} * G_1$$

and

$$V_2 = V_{CM} + \frac{V_D}{2} * G_1 \qquad (5)$$

Where Gain, $G_1 = 1 + (2*R_F/R_G)$

Equation 5 represent that only difference voltage term is amplified by gain and common mode voltage is passes input stage with unity gain.

The output of difference amplifier after the second stage can be describe by

$$V_0 = (V_2 - V_1)*G_2 \qquad \text{where } G_2 = R_2/R_1 \qquad (6)$$

by using equation 5&6 the transfer function of instrumentation amplifier can be expressed as:

$$\frac{V_0}{V_D} = G_1 * G_2 = G_{total} \tag{7}$$

Standard instrumentation amplifier using a unity gain difference amplifier in the output stage, however, can limit the input common mode range significantly [14]. The three op-amp IA suffers from a limited Common Mode Rejection ratio (CMRR) due to resistor mismatch [8]. It does not provide a good power noise tradeoff A switched-capacitor IA can be used to improve the CMRR, but it suffers from low input impedance. A CFIA can achieve better CMRR and input impedance as compared to three op-amp and Switched Capacitor IA.

3. Current Feedback Instrumentation Amplifier

Instrumentation Amplifier (IA) can be implemented in different ways. In the previous section we have discussed some of the commonly used topologies. Figure 3 shows block diagram of CFIA. The differential current (I_{in}) is calculated by converting differential input voltage (V_{in}) using the input trans-conductor ($g_{m,in}$). When feedback voltage V_{fb} is applied to feedback trans-conductor, it generates a differential current I_{fb}. Feedback voltage is an attenuated version of output voltage (V_{out}) achieved through a resistive network formed by $R1$ and $R2$. The amplifier output (A_{out}) maintains o/p voltage such that the sum of differential currents I_{fb} and I_{in} is zero under the steady state condition. The output voltage V_{out} is given by the following equation:

$$OutputVoltage(V_{out}) = \frac{g_{m,in}}{g_{m,fb}} . \frac{R_1 + R_2}{R_2} . V_{in} \tag{8}$$

$g_{m.,in}$ and $g_{m,fb}$ can be made equal to simplify the output voltage equation

$$OutputVoltage\ (V_{out}) = \frac{R_1 + R_2}{R_2} . V_{in} \tag{9}$$

This Current feedback topology achieves a high CMRR as compared to three op-amp topology. It is due to the input trans-conductor $g_{m,in}$, isolates the input common mode (CM) level by converting the V_{in} to I_{in}. Hence, the CMRR will be determined by the CMRR of input trans-conductor. Another advantage of CFIA compared to the three op-amp topology is that CFIAs can work in a large Common Mode Voltage Range (CMVR), which can include either of the supply rails [15].

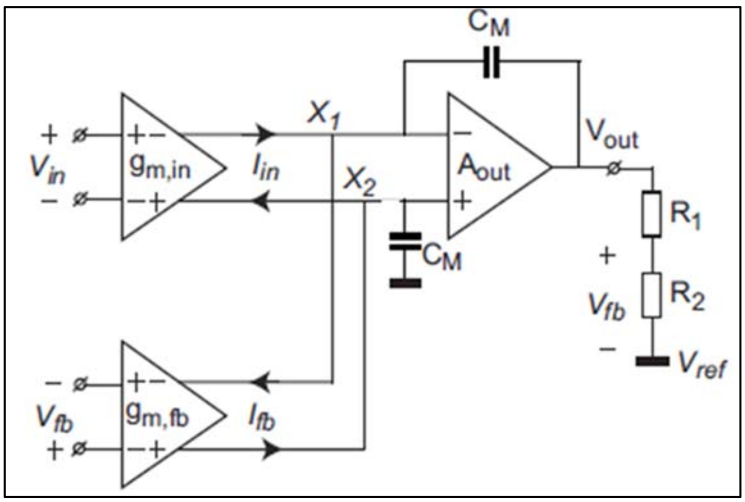

Fig 3: Current Feedback Instrumentation Amplifier (CFIA) [15]

In ideal amplifiers, when (V_{in+}-V_{in-}) =0, means the input differential signal is zero, the output differential signal is zero. However, in actual implementation, due to mismatching of register and transistor ($R1 \neq R2$ and $M1 \neq M2$), there is a finite DC voltage at the output even for zero input signal voltage. This DC voltage is referred to as offset. The mismatch in components can be due to variation in doping concentrations and lithographic errors.

Dynamic Offset Cancellation Technique for CMOS Amplifiers:

In case of CMOS amplifier offset, drift and flicker noise (1/f) are the dominant noise sources at lower frequencies. There are some techniques to reduce this kind of noise for offset reduction named as: Chopping, trimming and auto-zeroing. Trimming is basically works at the development phase to cancel the offset. Likewise auto-zeroing is based on sampling, in which offset is first measured and then it is subtracted in the upcoming clock phases. Last technique is chopping, based upon modulation technique in continuous time domain in which input signal as well as offset is modulated to different frequencies results chopper ripples at the output of amplifier circuit. Since both chopping and auto-zeroing are dynamic in nature to cancel the offset effect. These techniques are also useful in the reduction of offset drift and flicker noise over variation in time & temperature.

4. The State Of Art in CFIA

In the previous work many precision CFIAs have been designed, which use dynamic offset cancellation techniques discussed above to achieve a low offset and low noise performance with some other design parameters.

Table 1: Specifications of present state-of-the-art precision CFIA designs

Parameters	Teng'14 [16]	Sakunia'11 [11]	Pertijs'10 [9]	Witte'08 [15]
Technology	0.18 µm	0.5 µm	0.5 µm	0.8 µm
Technique for IA	Chopping	Chopping & Auto-zeroing	Chopping & Auto-zeroing	Chopping & Auto-zeroing
I/P Offset Voltage	17.6mV	4µV	3µV	5µV
CMRR	100 dB	122 dB	140 dB	143 dB
Absolute Gain Accuracy	-	±0.04%	±0.1%	±0.1%
Relative Gain	-	±0.003%	-	-
NEF	-	24	43	143
Gain Bandwidth	200 KHz	1 MHz	800 KHz	1 MHz
Input Voltage Noise	3.76µV/√Hz	27nV/√Hz	27nV/√Hz	142nV/√Hz
Supply Voltage	2.7 V	3.3-5.5 V	3.0-5.5 V	2.8-5.5 V
Supply Current	27.65 µA	483 µA	1700 µA	850 µA

Using dynamic offset cancellation techniques like chopper stabilized and auto-zeroing, the designs mentioned in table 1 achieve high CMRR, low input offset voltage as well as low input voltage noise. These designs [9, 11, 15, 16] are almost implemented with same offset compensation techniques with little variation in their structure. Like Witte'08 [15] achieve high CMRR compare to others but having little high offset at input to Sakunia'11 [11] and Pertijs'10 [9]. In case of input voltage noise [9, 11] gives least noise compare to others. This work targets to improve the performance in terms of offset & noise in a precision CFIA at high power efficiency, while maintaining the state-of-the-art offset and noise performance. The target specification to proceed this work in further research is shown in table 2.

Table 2: Target Specification

Parameters	Target specifications
Input Offset	< 3µV
Input Voltage Noise	< 27nV/√Hz
Gain Bandwidth Product	1 MHZ
CMRR	> 140 dB
Gain Error	< 0.01%
Temperature Range	-40°C to 125°C

5. Conclusion

In this paper, the designing concept for instrumental amplifier (IA) using different topology for low voltage and low power sensor applications is unveiled. The most emerging topology current feedback is discussed to design IA. While the basic building block of IA is a two-stage amplifier with Miller compensation, can be used in low power, low voltage High CMRR and PSRR. The circuit has been designed using different CMOS technology varying from 800nm to 180nm as shown in state-of-art. To reduce the noise of the instrumentation amplifier, different dynamic offset cancellation techniques is used. The main focus of this work is to introduce the beauty of IA for precise application since it needs to distinguish noise and the desired signal which is of small amplitude.

6. References

1. Menolfi C, Huang Q. A fully integrated, untrimmed CMOS instrumentation amplifier with sub-microvolt offset, IEEE J. Solid-State Circuits. 1999; 34(3):415-420.
2. Fan Q, Sebastiano F, Huijsing JH, Makinwa. A 1.8 W 60 nV/√Hz capacitively-coupled chopper instrumentation amplifier in 65 nm CMOS for wireless sensor nodes, IEEE J. Solid-State Circuits. 2011; 46(7):1534-1543.
3. Joachim Nagel H. Biopotential Amplifiers, the biomedical engineering handbook: Second Edition. Ed. Joseph D. Bronzino Boca Raton: CRC Press LLC, 2000.
4. Intersil AN. 1298: Instrumentation Amplifier Application Note. 2009, 1-35.
5. Hu Y, Sawan M. CMOS front-end amplifier dedicated to monitor very low amplitude signal from implantable sensors," Analog Integrated Circuit Signal Processing. 2002; 33:29-41.
6. Ahmed N, Hesham N. A low Power low noise Capacitively Coupled Chopper Instrumentation Amplifier in 134 nm CMOS for Portable Biopotential Acquisition Systems", IEEE Conference, 2013.
7. Rong Wu, Kofi Makinwa AA, Johan Huijsing H. A Chopper Current-Feedback Instrumentation Amplifier with a 1 mHz 1/f Noise Corner and an AC-Coupled Ripple Reduction Loop", IEEE Journal Solid-State Circuits. 2009; 44(12):3232-3243.
8. Wu R, Huijsing JH, Makinwa KAA. A Current Feedback Instrumentation Amplifier with a Gain Error Reduction Loop and 0.06 % Untrimmed Gain Error, IEEE Journal Solid State Circuits. 2011; 46:2794-2806.
9. Pertijs M, Kindt WJ. A 140 dB-CMRR current-feedback instrumentation amplifier employing ping-pong auto-zeroing and chopping", IEEE Journal Solid-State Circuits. 2010; 45(10):2044-2056.
10. Tang ATK. A 3µV-Offset operational amplifier with 20 nV/√ Hz input noise PSD at DC employing both chopping and auto-zeroing, IEEE ISSCC Digital Tech. Papers. 2002, 386-387.
11. Saket Sakunia F, Witte Pertijs M, Makinwa K. A Ping-Pong-Pang Instrumentation Amplifier with 0.04% Gain Error", Symposium on VLSI Circuits Digest of Technical Papers, 2011.
12. Teng Ong G, Pak Kwong Chan, A Power-Aware Chopper-Stabilized Instrumentation Amplifier for Resistive Wheatstone Bridge Sensors, IEEE Transaction on Instrumentation and Measurement. 2014; 63(9):2253-263.
13. Anton Bakker, Kevin Thiele, Johan Huijsing H. A CMOS Nested Chopper Instrumentation Amplifier with 100 nV Offset, IEEE Journal Solid State Circuits. 2000; 35(12):1877-1883.
14. Thomas Kugelstadt. Getting the most out of your instrumentation amplifier design", Analog Applications Journal, Texas Instruments Incorporated, Texas, USA. 2005, 25-30.

15. Witte JF, Huijsing JH, Makinwa KAA. A chopper and auto-zero offset-stabilized CMOS instrumentation amplifier, IEEE Journal VLSI Circuits. 2009, 210-211.
16. Teng Ong G, Pak Kwong Chan. A Power-Aware Chopper-Stabilized Instrumentation Amplifier for Resistive Wheatstone Bridge Sensors, IEEE Transaction on Instrumentation and Measurement. 2014; 63(9):2253-263.