International Journal of Multidisciplinary Research and Development
Online ISSN: 2349-4182, Print ISSN: 2349-5979, Impact Factor: RJIF 5.72
www.allsubjectjournal.com
Volume 4; Issue 7; July 2017; Page No. 335-344

A three-level quasi-two-stage three-phase PFC converter

[1] Bhagyashri C Chavan, [2] Netra M Lokhande

[1] Me Student at Tssm's Bscoer, Electrical Engineering, Savitribai Phule Pune University, Pune, Maharashtra, India
[2] Professor at Tssm's Bscoer, Electrical Engineering, Savitribai Phule Pune University, Pune, Maharashtra, India

Abstract
This paper presents a three-level two-stage Three-phase power factor correction (PFC) converter that has flexible output voltage and improved conversion efficiency. The proposed PFC converter features sinusoidal input current, three-level output characteristic, and a wide range of output DC voltages, and it will be very suitable for high power applications where the output voltage can be either lower or higher than the peak AC input voltage, e.g. plug-in hybrid electric vehicle (PHEV) charging systems.
Moreover, the involved DC/DC buck conversion stage may only need to process partial input power rather than full scale of the input power, and therefore the system overall efficiency can be much improved. Through proper control of the buck converter, it is also possible to mitigate the double-line frequency ripple power that is inherent in a three-phase AC/DC system, and the resulting load end voltage will be fairly constant. The dynamic response of this regulation loop is also very fast and the system is therefore insensitive to external disturbances. In this paper, the operation of the new converter is explained, its features and design are discussed in simulation & experimental results, and its operation is confirmed with experimental results obtained from a prototype.

Keywords: PFC converter, three level characteristics, active power decoupling, conduction losses, current regulation, power factor correction, harmonic distortion, discontinuous conduction mode

1. Introduction
Three phase rectifiers have a wide range of application many industrial as well as residential applications like electrochemical processes, arc furnaces, adjustable speed drives, variable speed drive, electric vehicle (EV) chargers, and power supplies for consumer electronics. With the ever increasing use of power electronic equipment, employing rectifiers is unavoidable in many applications. The major problem with the conventional rectifiers is harmonic pollution [1]. Today's standards like International Electro-technical Commission (IEC) 61000-3-2 limit the harmonics produced by these devices as long as their power ratings exceed 75W [2]. Therefore, to satisfy the standards, power-factor-correction (PFC) converters are used for ac–dc conversion. The conventional PFC converter is a boost converter, and thus, the output voltage must be greater than the input voltage [3]. In spite of this problem, this converter is widely used because of its simplicity.
The most common approach to PFC is to use two-stage power conversion schemes. These two-stage schemes use a front-end ac–dc converter stage to perform ac–dc conversion with PFC with the output of the front-end converter fed to a back-end dc–dc converter stage that produces the desired isolated dc output voltage [4]. The front-end converter for various applications must achieve high power factor, low harmonic distortion, high efficiency, high power density, high reliability and low electromagnetic interference (EMI) noise. To reduce the cost of the front-end converter, the PFC stage must be inexpensive, while still complying with standards for harmonic distortion.
That the first stage of each module is used to perform the PFC function to meet harmonic current standards such as the IEC 61000-3-2, while the second-stage DC/DC converter regulates the DC output voltage of the system and guarantees system current sharing.
In large number of applications, like offline low-voltage power supplies, where it is preferred to have the PFC output voltage lower than the input ac voltage, a buck-type converter is required. However, the input current of buck converter is discontinuous, and to filter this current, another passive filter must be used at the buck converter input. Presently, Three-phase power factor correction (PFC) converters are a very popular solution to ensure the compliance of such regulations because of their simplicity, cost effectiveness and good current shaping capability. However, most of the existing Three-phase PFC converters are of boost type and can only provide an output voltage that is higher than the peak voltage of the AC input [5-6]. Wide range of output voltage is indeed desired in some applications like in plug-in hybrid electric vehicle (PHEV) charging systems where the terminal voltage of battery packs may vary between 100V to 600V, In this case, a second stage DC/DC buck converter has to be implemented to further step down the PFC output voltage, which undoubtedly decreases the system overall efficiency.

2. Literature Review
In order to provide flexible DC output voltages, PFC converters with buck-boost capabilities have been studied in the literatures and they are usually based on buck-boost, fly back, Cuk, and Single-ended primary inductance converter (SEPIC) topologies, and can be derived in both non-isolated and isolated versions [7-9]. A common problem for these topologies is that there is no direct energy transfer path during power conversion and all input power must be processed by active switches and stored by intermediate passive components (either inductors or capacitors) before being

supplied to the end loads [10]. This indicates that the components will be working under increased voltage/current stresses, which may consequently lead to decreased power density and conversion efficiency.

In order to improve the performance of Cuk and SEPIC based PFC topologies, their bridgeless variants have recently been proposed in [11-13] with most of them being operated in discontinuous conduction mode (DCM). In this case, the PFC converter can be constructed with less semiconductor switches and the on-state conduction losses can be reduced. The switching losses are reduced as well due to their DCM operation. However, the main power switches in these bridgeless topologies are still under high voltage stress and the DCM operation also implies that they are only suitable for relatively low power applications because of the high peak current in the boost inductor.

In view of this, AC/DC converters with direct buck capability are highly desired in high power PHEV battery charger applications and a buck type PFC topology, named as Swiss Rectifier has already been proposed in [14, 15] for three-phase AC/DC systems.

The bridgeless derivative of the buck PFC was also proposed in [18] to further improve its conversion efficiency. Unfortunately, such buck PFC converters may inherently subject to a so-called "dead angle" limitation when the input voltage is lower than the output voltage. The AC side input current cannot be regulated to be purely sinusoidal and unity power factor is not achievable. An improved buck PFC converter with high power factor is proposed in [19], where an auxiliary switch and two diodes are added in the circuit to provide current regulation during the "dead angle" period. Although the power factor can be improved, the input current waveform is still not sinusoidal and therefore, they may only be suited for low power applications (less than 1kW), e.g. laptop adapter, TV sets power supplies. Another buck PFC converter with power decoupling capability has recently been proposed in [20], and it features high quality input current as well as ripple free output voltage. However, the limitation of this topology is that, its output voltage must be lower than half of the peak AC input voltage

Previously proposed three-phase single-stage ac–dc converters, however, have at least one of the following drawbacks that have limited their widespread use.

1. They are implemented with three separate ac–dc single-stage modules [13, 14].
2. The converter components are exposed to very high dc bus voltages so that switches and bulk capacitors with very high voltage ratings are required [16-17].
3. The input currents are distorted and contain a significant amount of low-frequency harmonics because the converter has difficulty performing PFC and dc–dc conversion simultaneously [16].
4. The output inductance must be very low, which makes the output current to be discontinuous. This results in a very high output ripple so that secondary diodes with high peak current ratings and large output capacitors to filter the ripple are needed [13, 17].
5. Most of them are in discontinuous conduction mode at the input and need to have a large input filter to filter out large high-frequency harmonics [13, 15, 17, 22]

This paper presents a new interleaved three-phase two-stage rectifier that does not have any of these drawbacks. This topology has a high efficiency single-phase PFC converter that features sinusoidal input current, three-level output characteristic and flexible output DC voltage. Its attractiveness is that, in case of buck operation mode, the embedded bidirectional DC/DC converter may only need to process partial input power rather than full scale of the input power, and therefore its conversion efficiency can be much improved as compared with the conventional two-stage solution. Also, the PFC stage exhibits three-level output voltage, and the dV/dt across the switches are reduced, so as the switching losses. An added benefit of this converter is that, the fluctuating 100/120Hz harmonic power in the single-phase system can be almost diverted into the dc-link capacitor through proper control design, and the load voltage will be fairly constant.

In this paper, the operation of the new converter is explained, its features and design are discussed and its operation is confirmed with simulation & experimental results obtained from a prototype.

3. System Description

The circuit diagram of the proposed three-phase AC/DC converter is shown in Fig. 1, which consists of a standard diode rectifier bridge, a three-level PFC, and a bidirectional DC/DC converter. The PFC stages are connected with two DC buses, i.e. a low voltage DC bus that directly supplies power to the load, and a high voltage DC bus that supports three-level operation and absorbs system harmonic power. Power Factor increases in two stages, First stage consist of two switching device Q_1 & Q_2 (MOSFET's).Q_1 & Q_2 for charging & discharging purpose. Diode D_1 for reverse protection purpose & one inductor L_{in} which is inrush current limiting inductor. Diode D_2 also for reverse current protection. C_L & R_L loads of stage first stages. Second stage consists of another one inductor L_{dc} through which center out-put is given to second stage. It consist of another switching device Q_3 & Q_4, for providing smooth out put voltage, Q_3 & Q_4 provide ripple power consumption during both operating period. CH is the high output load. In order to control the PFC & intermittent operation of Q_1 & Q_2 impose the disturbance to the system, PI controller i.e. AVR microcontroller is used. For isolation purpose opt coupler is used. The IRF630 is high voltage, high speed power MOSFET drivers with independent high and low side referenced output channels. The floating channel can be used to drive an N-channel power MOSFET in the high side configuration which operates up to 500 or 600 volts.

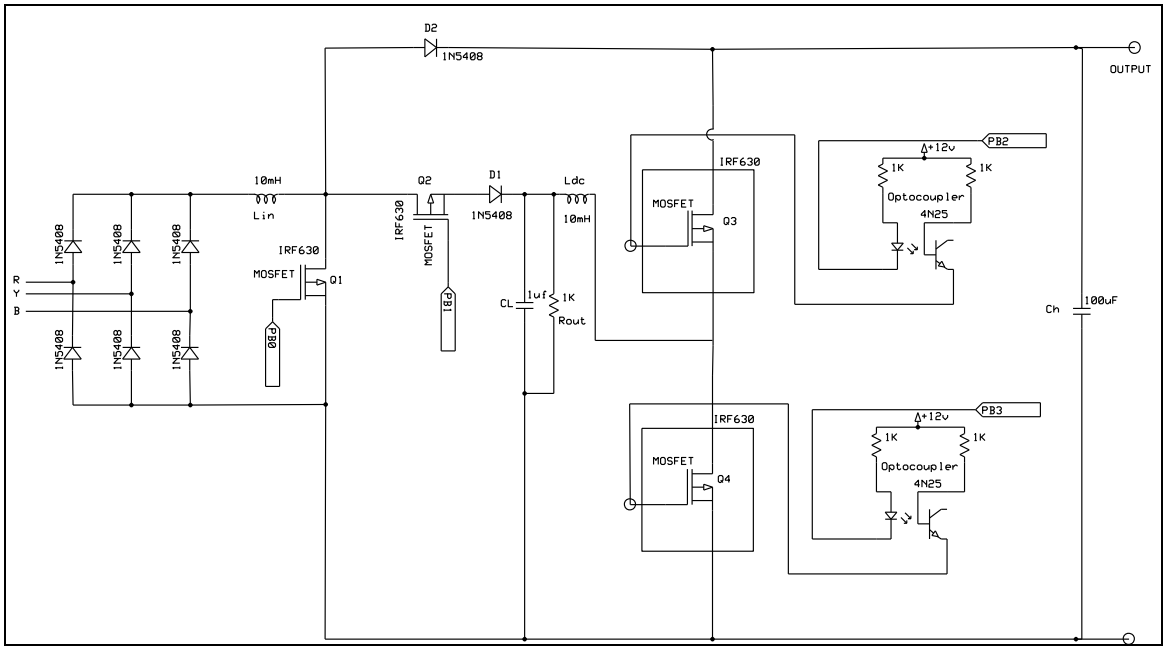

Fig 1: Circuit diagram of the proposed three-level PFC converter

4. System Operation

4.1 Operating stage first

The proposed three-level PFC has a wide range of output voltages and it can function as either a buck or a boost converter. During buck operation, there are two operation modes for Q1 and Q2. When the low DC bus voltage or simply the load voltage *VL* is higher than the instantaneous input voltage *Vin*|sin*ωt*|, where *Vin* is the peak value of input voltage and *ω* is the fundamental angular frequency, Q2 will be always on. Q1 and D1 then form up a standard boost PFC that directly converts input power for DC load consumption, and the converter pole voltage *VAB* will be changed between 0 and *VL*. In order to realize PFC function, the duty cycle of Q1 should comply with,

$$d_1 = 1 - \frac{V_{in}\,|\sin \omega t|}{V_L} \qquad (1)$$

It is the basic equation for a boost PFC. It should be noted that, in this operation period, Q3 and Q4 of the buck converter theoretically do not need to switch because all input power can be directly supplied into the load through D1 and Q2. However, in order to obtain a smooth output voltage, Q3 and Q4 still need to work and provide ripple power compensation during this operation period.

4.2 Operating stage second

In the second operation interval when V_L is less than *Vin*|sin*ωt*|, Q1 remains off. Q2 and D2 will modulate and form up another boost PFC. In this case, the converter pole voltage V_{AB} is changing between V_L and the high DC bus voltage V_H. Again, to ensure sinusoidal input current and unity power factor, the duty cycle of Q2 must comply with,

$$d_2 = 1 - \frac{V_{in}|\sin\omega t| - V_L}{V_H - V_L} \qquad (2)$$

Intuitively, when D2 is conducting, excessive input power will be flowing into the dc-link capacitor C_H and this high bus voltage will be subsequently stepped down by the bidirectional DC/DC converter to cater for load consumption, and this is the root reason that why the DC/DC converter may only process partial input power and higher conversion efficiency can be obtained through the proposed topology. The idealized operating waveforms during these two modes presented in Fig. 2. In order to ensure smooth transition between the low and high voltage level commutations, an offset is injected into the carrier of the pulse-width modulation (PWM) for Q2 as shown in Fig. 2. As a result, a unified reference signal *Vm* can be derived to simultaneously modulate Q1 and Q2, which is written as,

$$V_{in}(t) = \begin{cases} 1 - \dfrac{V_{in}|\sin\omega t|}{V_L} & ,V_{in}|\sin\omega t| \le V_L \\ \dfrac{V_L - V_{in}|\sin\omega t|}{V_H - V_L} & ,V_{in}|\sin\omega t| > V_L \end{cases} \qquad (3)$$

Compared with the conventional boost PFC, the proposed converter will have slightly higher conduction losses because of the series connection of Q2 and D1. However, its switching losses can be greatly reduced due to its three-level output that splits the high DC bus voltage into two low voltage portions. Moreover, efficiency gain from the DC/DC converter is also significant because it only converts the input power that flow through D2.

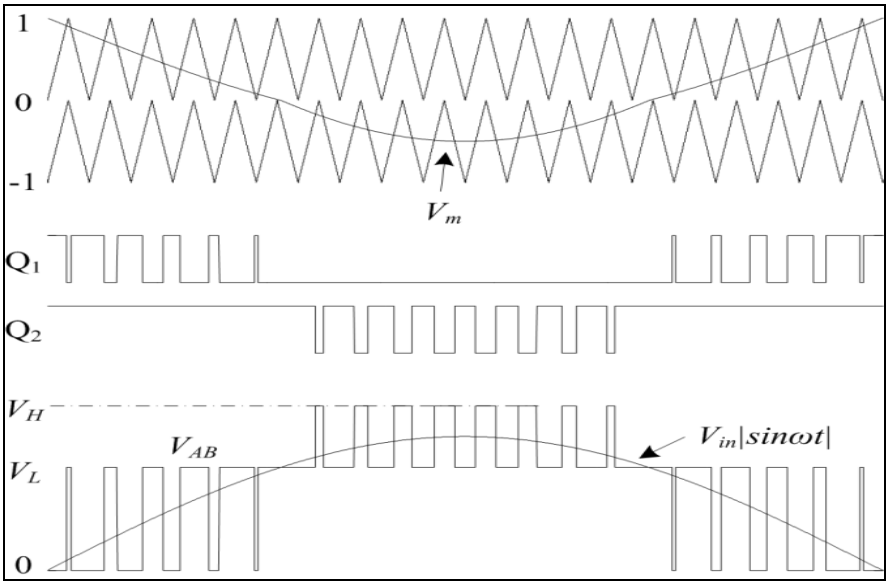

Fig 2: Idealized operating waveforms for the proposed three-level PFC converter.

To estimate the percentage of input power that is converted by this buck stage, it is assumed that the power converter is lossless and harmonic free. In this case, the instantaneous input power from AC side will be,

$$P_{In} = V_{in}|\sin\omega t|.I_{in}|\sin\omega t| = \frac{V_{in}I_{in}}{2}(1-\cos 2\omega t) \quad (4)$$

Iin is the peak value of boost inductor current. If the PFC is commutating at high voltage levels, part of the input power will be directly supplied into the load when Q2 is on, and it can be found as,

$$P_{batt_H} = I_{in}|\sin\omega t|.d_2.V_L = I_{in}|\sin\omega t|\left(1-\frac{V_{in}|\sin\omega t|-V_L}{V_H-V_L}\right)$$
$$= V_L I_{in}|\sin\omega t|\left(\frac{V_H-V_{in}|\sin\omega t|}{V_H-V_L}\right) \quad (5)$$

Plotting (4) and (5) will give rise to the time domain waveforms of power distribution shown in Fig. 3, and it is clear that the shaded area enclosed by *pin* and *pbatt_H* indicates the active power *pdc* that needs to be processed by the buck converter.

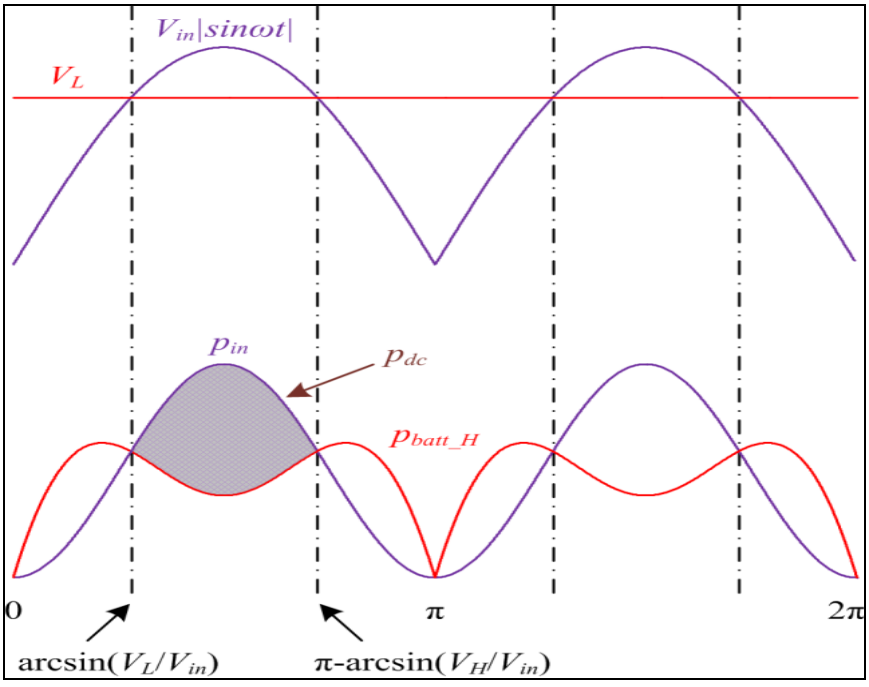

Fig 3: Instantaneous power distribution in the PFC converter and the buck converter, given fixed gird voltage, output voltage, and dc-link voltage.

In addition to the buck operation, the proposed PFC can also function as a boost and this operation mode is triggered when *VIN*<V_L<V_H. In this case, the modulation scheme discussed above is still applicable. According to (2), the duty cycle of Q_2

will be greater than 1, implying that Q_2 is always on. Therefore, the proposed circuit is simplified as a conventional two-level PFC that is comprised of Q_1 and D_1 only, and the buck converter is only used for ripple power compensation.

5. System Controller Design

The control system of the proposed three-level AC/DC converter will be relatively more complicated than that of a conventional boost PFC, because it requires at least two voltage control loops to regulate the output voltage V_L and the dc-link voltage V_H, respectively. Also, the intermittent operation of Q_1 and Q_2 imposes a disturbance to the system, and a fast control loop must be designed to reject this periodic disturbance. In order to realize these control objectives, two independent control loops are designed for controlling the PFC stage.

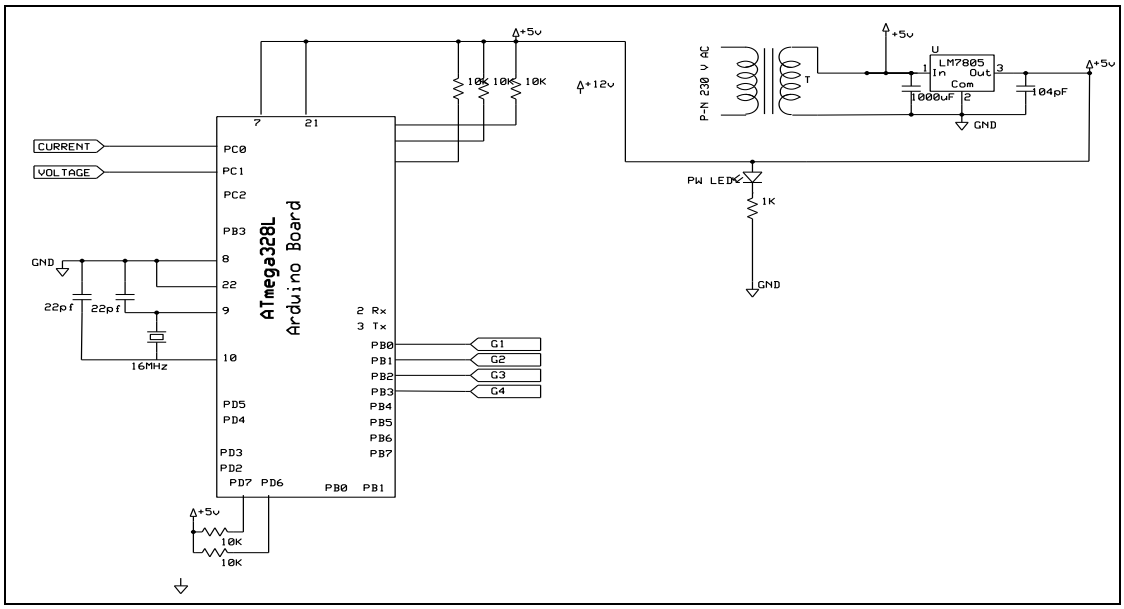

Fig 4: Circuit diagram of controller circuit for PFC converter.

Fig. 4 consist of PI controller, microcontroller AVR require 5volt Supply, which is provides by 230/12 volt transformer, this 12 volt transformer output voltage can be regulated in 5 volt by the voltage regulator. Gate pulses to Q_1, Q_2, Q_3 & Q_4 can be provides from the out-put port of microcontroller PB0, PB 1, PB 2, PB3.

In order to realize these control objectives, must be designed to reject this periodic disturbance. Two independent control loops are designed for controlling the PFC stage and the buck stage, respectively

5.1 PFC Converter Control

A classic cascaded control structure is employed to regulate the PFC converter. Its outer voltage control loop is tasked at balancing input and output power, and the dc-link voltage V_H is chosen as the control variable because the charging power into the dc-link capacitor C_H is directly proportional to input power as long as V_L, *Vin*, and V_H are fixed. This voltage control loop will also maintain the average value of V_H to be constant, whereas its instantaneous value is not necessary to be constant, because the dc-link capacitor C_H has to absorb the double line frequency harmonic in this single-phase system. The control loop is therefore of slow response and its control bandwidth is set below 20Hz as per usual design, and this is realized by tuning the parameters of a proportional-integral (PI) regulator *Gv*(*s*) as follow,

$$G_v(s) = K_{pv}\left(1 + \frac{1}{\tau_v s}\right). \quad (6)$$

Where *Kpv* is the proportional gain to adjust control bandwidth, and τv is the time constant of the integral term to achieve high DC compensation gain.

In order to prevent the dc-link ripple voltage from distorting the reference of inner current control loop, a second order notch filter tuned at 2ω is added at the output of the PI regulator.

$$G_{notch}(s) = \frac{s^2 + 2\omega^2}{s^2 + K_2 s + 2\omega^2} \quad (7)$$

Where K_2 is a coefficient that determines the quality factor of this notch filter. Large K_2 can give rise to more attenuation of double line frequency harmonic, but in the meantime, it may reduce the phase margin of the control loop, and thus deteriorate system dynamic response. The transfer function of duty cycle-to-inductor current *Gid_PFC*(*s*) can be simply regarded as a first order inertial element in the high frequency through the small signal modeling approach, and in this case it can be written as,

$$G_{id\_pfc}(s) = \frac{I_{in}(s)}{d_{pfc}(s)} = \frac{V_{dc}}{sL_{in}} \quad (8)$$

where *Vdc* is the output voltage that may change between *VL* and (V_H-V_L), depending on the operation mode of the PFC. It is worth noting that this voltage change is undesired in the system, because it may give rise to a variable bandwidth of the current control loop and affect its regulation performance. In

order to have a fixed control bandwidth for the inner current loop, a dynamic gain compensator is implemented as shown in the right bottom part of Fig. 5, and an upper saturation is set to limit the gain value *Gdy* in case that V_L is approaching V_H. In this case, the inner current loop can be easily controlled by another PI regulator,

$$G_c(s) = K_{pc}\left(1 + \frac{1}{\tau_c s}\right) \tag{9}$$

where *Kpc* is its proportional gain and *τc* is the time constant. These two coefficients should be tuned such that the bandwidth of the current control loop is around one tenth of the system switching frequency. In order to achieve accurate current tracking and make the control system robust against line voltage change, a duty cycle feed-forward control scheme is also implemented in the current loop.

5.2 Buck Converter Control

As mentioned earlier, the output voltage of the buck converter should be as constant as possible because it is directly connected to end loads. Therefore, a single voltage control loop is designed for this power stage to expedite its dynamic response and also to save a current transducer. Another reason for pursuing fast response of this voltage control loop is that it has to reject the periodic disturbance induced by its intermittent operation. the equivalent load resistance R_{load} is much larger than the ESRs and the filter inductance L_{dc}, the control duty cycle-to-output voltage transfer function $G_{vd\_dc}(s)$ of the bidirectional buck converter can be derived as,

$$G_{vd\_dc}(s) = \frac{V_L(s)}{d_{dc}(s)} = V_H \frac{1+\frac{s}{\omega_z}}{1+\frac{s}{Q\omega_0}+\frac{s^2}{\omega_0^2}} \tag{10}$$

where *ωo* is the LC resonant frequency introduced by the output filter. *RCL* is the ESR of the output capacitor C_L and it introduces a zero *ωz* in the open loop gain. R_{Ldc} is the ESR of the boost inductor and these two ESRs together determine the quality factor *Q* of this second order system and they can provide damping effect to the LC resonance. Using the parameters listed in Table I, the system is closed-loop control system is inherently stable even a simple proportional gain is used. However, if the crossover frequency of this control loop is tuned to be less than one tenth of the switching frequency, e.g. 1 kHz the system phase margin is only 17°, which is obviously insufficient and may cause transient oscillations. Furthermore, this system has limited DC gain, and its steady-state tracking error may not be zero.

In order to solve these issues, a type III compensator is then designed to control this buck converter and its standard form can be written as,

$$G_{dc}(s) = \frac{K_{dc}\left(1+\frac{s}{\omega_{z1}}\right)\left(1+\frac{s}{\omega_{z2}}\right)}{s\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)} \tag{11}$$

Clearly, the integral term is to produce infinite DC gain for zero steady-state tracking error, and the two zeros ωz_1 and ωz_2 should be placed around the LC resonance frequency *ωo* so that phase boost can be obtained. The first high frequency pole *ωp1* is to cancel the ESR zero introduced by the output capacitor, while the other pole ωp_2 acts as a low pass filter (LPF) which increases gain attenuation at high frequencies. A common way is to set ωp_2 to be around half of the switching frequency. By using type III compensator confirms its stable operation and fast transient response.

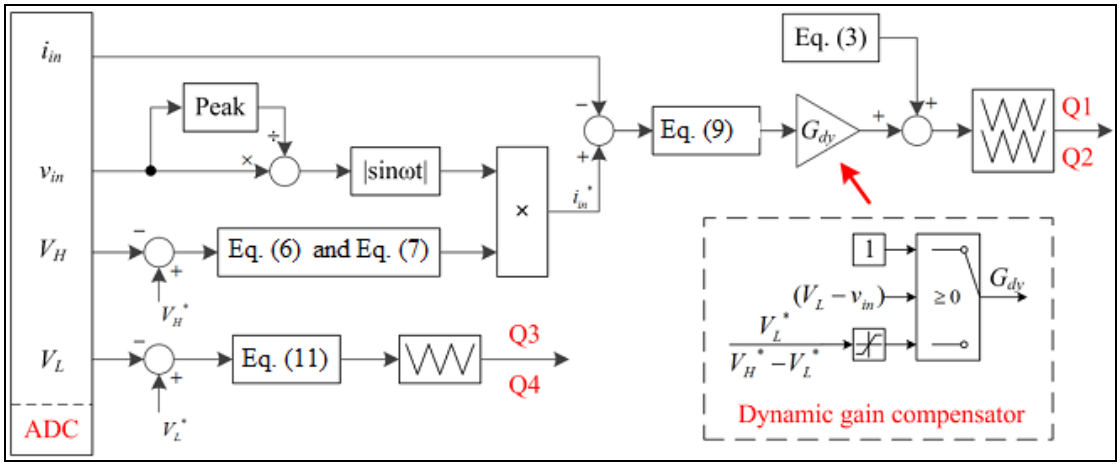

Fig 5: Overall control block diagram for the proposed three-level PFC converter.

6. Simulation & Simulation Result

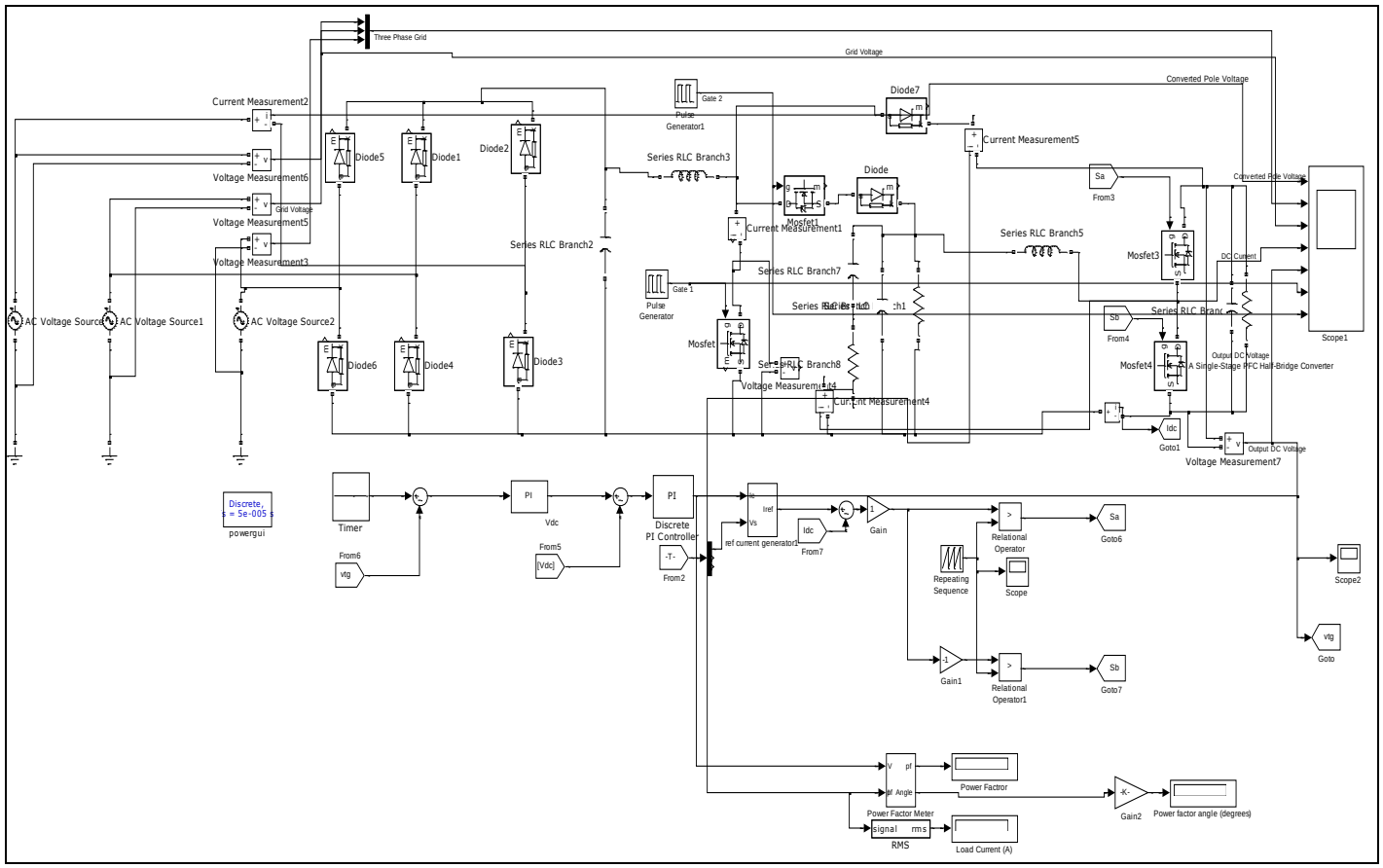

Fig 6: Simulation for Three level-Quasi-Two Stage PFC converter

Simulation study was carried out in Matlab/Simulink environment and the circuit parameters are listed in Table 1. Simulation for Three level-Quasi-Two Stage PFC converter is shown in Fig.6. The steady-state operation waveforms are presented in Fig.7. It can be seen that Q_1 and Q_2 operate alternatively and may produce the desired three-level converter pole voltage V_{AB}. The high level bus voltage is not constant because the dc-link capacitor needs to absorb the system double line frequency harmonic. This fluctuation voltage has basically no impact to the regulation of the boost inductor current, because it can be easily compensated by the fast current control loop. Thanks to the feed-forward mechanism of the open loop duty cycle, the grid current is almost sinusoidal and in phase with the grid voltage, and its ripple component is very small because of the three-level output voltage.

Table 1: Circuit Parameters used for Simulation and Experiment

Description	Symbol	Value
Grid voltage	V_g	440 √2 V
Line frequency	f_g	50 Hz
Output voltage	V_H	230 V
Switching frequency	f_{sw}	12.5.KHz
Nominal load	R_{load}	2.2 KΩ
Inductance	L_{in}/L_{dc}	0.66 mH
ESR of Inductor	R_{Lin}/R_{Ldc}	0.0011Ω
Capacitance	C_L/C_H	25 µF
ESR of capacitors	R_{CL}/R_{CH}	23.99Ω

As mentioned before, the buck converter theoretically does not need to switch when D_2 is blocking. However, in order to deal with the system harmonic power and ensure constant load voltage, the buck converter still has to work during this operation mode.

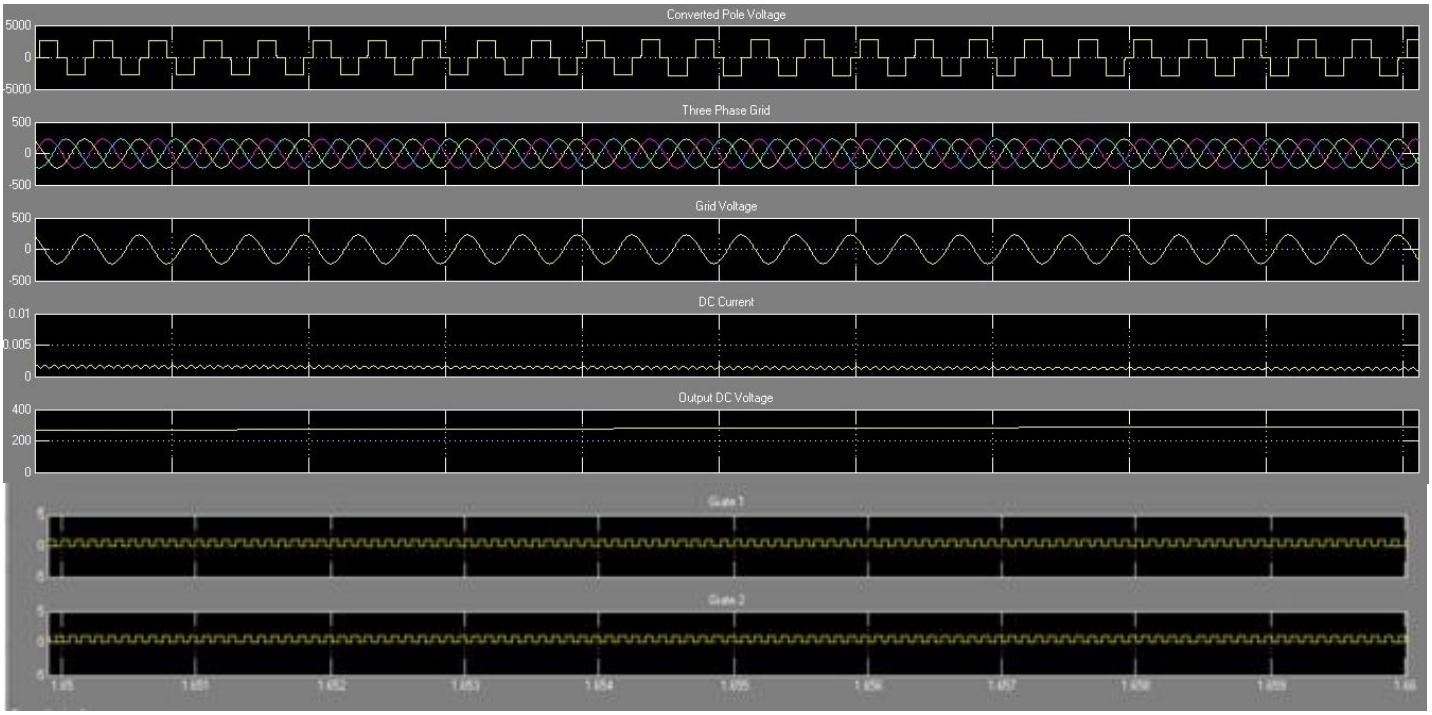

Fig 7: Simulation Steady state waveform under 430/2 KW operation, Converted pole voltage, three phase grid, grid voltage, output DC voltage, Gate pulses respectively.

7. Hardware Result

A 2kW prototype circuit was built in the laboratory for experimental validation of the proposed PFC converter and the circuit parameters are basically the same as those used in simulation, despite some very slight differences due to the tolerance of passive components. The key active and passive components used for the tested prototype are summarized in Table 2.

Table 2: Key Components Used for the Experimental Prototype

Component	Description
Diode Rectifier bridge	IN5408
Q1….Q4/D1/D2	IN4007-8
Lin/Ldc	0.66 mH,2*18/20W, Core, Crompton Greaves
CL/CH	25 µf /440 VAC, HITRON Capacitor

The proposed topology was first tested with standard 430V/50Hz high line AC input and its corresponding steady-state experimental waveforms are presented in Fig. 8 & 9. It is obvious that they can match well with those simulated ones presented in Fig. 7. It should be noted that there is very slight current distortion during the mode transition period, and this is due to the limited compensation gain of the controller.

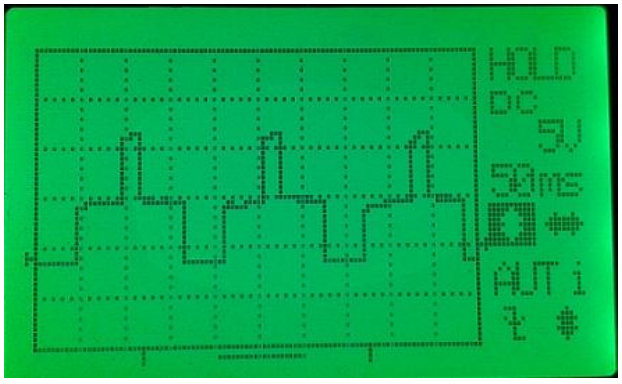

Fig 8: Converter Pole Voltage

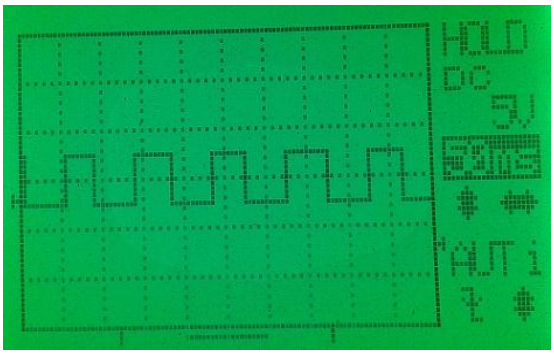

Fig 9: Gate pulses

The load transient can be handled by the high voltage bus and the output voltage remains undisturbed. In order to examine the line frequency ripple component in the output voltage, its spectrum is plotted in Fig. 10 and compared with that of the high DC bus. From Fig. 10, it is clear that the high DC bus can absorb most of the second order harmonics and therefore, the load voltage can be kept as ripple free during both steady-state and dynamic process.

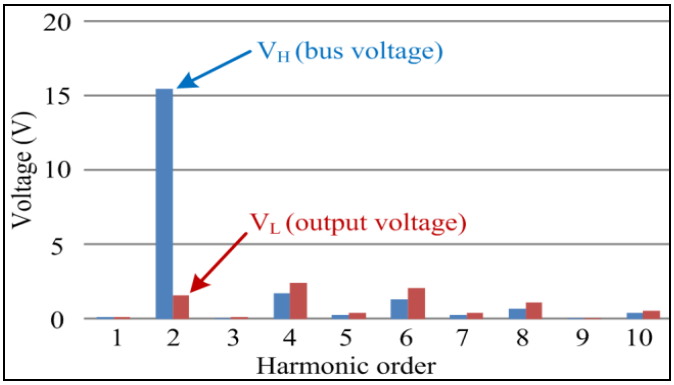

Fig 10: Harmonic contents of the output voltage and high DC bus voltage under 440V/2kW operation.

The proposed PFC converter is also compared with a conventional two-stage solution, i.e. a boost PFC cascaded with a DC/DC buck converter and its circuitry is obtained by removing D_1 and Q_2 shown in Fig. 1. Therefore, the proposed three-level PFC will have higher cost than the conventional one, and it is complicated with one fast recovery diode (D_1), one switch (Q_2) and one isolated gate driver. The remaining active and passive components in the two-stage PFC are exactly the same as those in the proposed one and therefore, a fair performance comparison can be conducted.

The efficiency tests were performed by a Fluke Norma 5000 power analyzer. Different tests under universal input voltage conditions (85Vrms to 265Vrms) were conducted for the two topologies. The output voltage and load power were fixed at 230V and 2kW, respectively, and the recorded efficiency curves are presented in Fig. 11. As shown, the proposed PFC features higher efficiency than the conventional one under all input conditions. During standard 230V high line operation, 1% efficiency improvement can be obtained over the entire load range and this confirms the superior performance of the proposed topology.

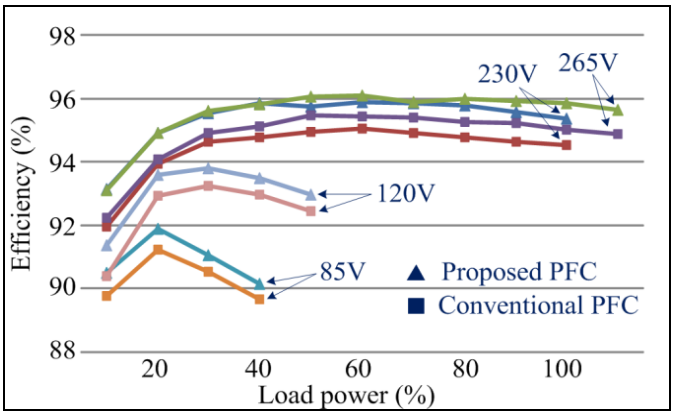

Fig 11: Efficiency curves of the proposed PFC converter under universal input voltages, shown in comparison with the conventional two-stage solution.

In addition to the efficiency versus input voltage curves, the efficiency versus output voltage curve is also plotted in Fig. 12, and in this test, the converters were operated with 430V input voltage and nominal load power. Fig. 12 shows that the proposed PFC can maintain much higher efficiency when the output voltage is low. However, as the output voltage increases, the efficiency improvement will be less significant because the proposed PFC essentially becomes equivalent to the conventional two-stage PFC and the characteristic of three-level switching is lost.

It should be noted that the power losses induced by the gate drivers were not included in the efficiency measurement. Since the required gate charge is low and the adopted switching frequency is also relatively slow, these power losses are insignificant to the system overall efficiency and the performance comparison presented above is still reasonable.

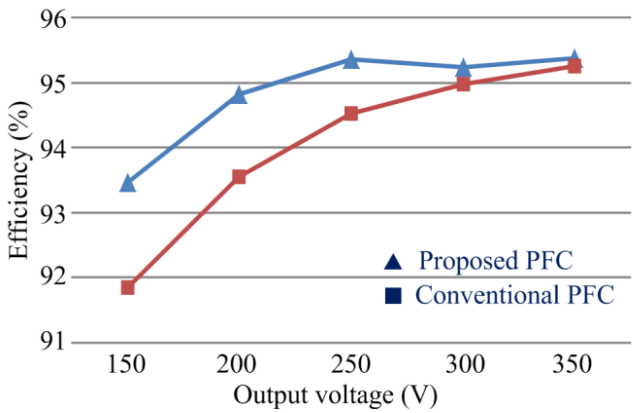

Fig 12: Efficiency curve of the proposed PFC converter under different output voltages, shown in comparison with the conventional two-stage solution.

8. Application

1. It has flexible output voltage and can be used for single-phase PHEV charger applications, where the battery voltage can be either lower or higher than the peak AC input voltage.
2. Used to reduce conduction losses.
3. Used in industries which have low power factor problems.
4. It is also used for low-output voltage applications, such as telecommunication or computer industry.
5. Used to improve Power factor & reduce total harmonic distortion.

9. Conclusion

In this paper, A three-level quasi two-stage three phases PFC converter is presented.

1. It has flexible output voltage and can be used for single-phase PHEV charger applications, where the battery voltage can be either lower or higher than the peak AC input voltage.
2. The proposed converter features high quality input current, three-level output voltage, and improved conversion efficiency.
3. By designing a fast regulation loop for the buck converter, the inherent fluctuating power issue in single phase systems can also be resolved, and the load voltage will be fairly constant and insensitive to load changes and external disturbances.
4. Moreover, a dynamic gain compensator is implemented in the current control loop and in this case, its control bandwidth can be kept relatively constant irrespective of the DC bus voltage change during two different operation modes. Therefore, the grid current can be well regulated with low THD and high power factor.
5. The proposed PFC may have 1% efficiency gain under

high line operation as compared to a conventional cascaded two-stage solution.

6. This efficiency improvement is partly contributed by the reduced switching voltage in the PFC stage, and also partly by the reduced power conversion in the DC/DC buck stage.

10. References

1. Singh B, Garg V, Bhuvaneswari G. An input current wave shaping AC-DC converter for rectifier loads, J. Power Electron. 2008; 8(1):1-9.
2. Electromagnetic Compatibility (EMC)-Part3: Limits-Section 2: Limits for Harmonic Current Emissions (Equipment Input Current < 16 A Per Phase), IEC Standard 61000-3-2, 1998.
3. Kazerani M, Ziogas PD, Joos G. A novel active current wave shaping technique for solid-state input power factor conditioners, IEEE Trans. Ind. Electron. 199; 38(1):72-78.
4. Tamyurek B, Torrey DA. A three-phase unity power factor single stage AC–DC converter based on an interleaved flyback topology, IEEE Trans. Power Electron. 2011; 26(1):308-318.
5. Musavi F, Eberle W, Dunford WG. A high-performance single-phase bridgeless interleaved PFC converter for plug-in hybrid electric vehicle battery chargers, IEEE Trans. Ind. Appl. 2011; 47(4):1833-1843.
6. Musavi F, Edington M, Eberle W, Dunford WG. Evaluation and efficiency comparison of front end AC-DC plug-in hybrid charger topologies, IEEE Trans. Smart Grid. 2012; 3(1):413-421.
7. Moo CS, Lee KH, Cheng HZ, Chen WM. A single-stage high-power-factor electronic ballast with ZVS buck–boost conversion, IEEE Trans. Ind. Electron. 2009 56():1136-1146.
8. Watson R, Hua GC, Lee FC. Characterization of an active clamp flyback topology for power factor correction applications, IEEE Trans. Power Electron. 1996; 11(1):191-198.
9. Zane R, Maksimovic D. Nonlinear-Carrier control for high-power-factor rectifiers based on up-down switching converters, IEEE Trans. Power Electron. 1998; 13(2): 213-221.
10. Chen J, Maksimovic D, Erickson RW. Analysis and design of a low-stress buck-boost converter in universal-input PFC applications, IEEE Trans. Power Electron. 2006; 21(2):320-329.
11. Mahdavi M, Farzanehfard H. Bridgeless SEPIC PFC rectifier with reduced components and conduction losses, IEEE Trans. Ind. Electron. 2011; 58(9):4153-4160.
12. Ismail EH. Bridgeless SEPIC rectifier with unity power factor and reduced conduction losses, IEEE Trans. Ind. Electron. 2009; 56(4):1147-1157.
13. Fardoun AA, Ismail EH, Sabzali AJ, Al-Saffar MA. New efficient bridgeless Cuk rectifiers for PFC applications, IEEE Trans. Power Electronics. 2012; 27(7):3292-3301.
14. Soeiro T, Friedli T, Kolar JW. Swiss Rectifier: A novel three-phase buck-type PFC topology for electric vehicle battery charging, in Proc. 26th IEEE Appl. Power Electron. Conf. Exp. 2012; 5(9):2617-2624.
15. Soeiro T, Friedli T, Kolar JW. Design and implementation of a three-phase buck-type third harmonic current injection PFC rectifier SR," IEEE Trans. Power Electronics. 2013; 28(4):1608-1621,.
16. Park JH, Cho B-H. The zero voltage switching (ZVS) critical conduction mode (CRM) buck converter with tapped-inductor, IEEE Trans. Power Electron. 2005; 20(4):762-774.
17. Wu X, Yang J, Zhang J, Xu M. Design considerations of a high efficiency soft-switched buck AC-DC converter with constant on-time (COT) control, IEEE Trans. Power Electron. 2011; 26(11):3144-3152.
18. Jang Y, Jovanovic MM. Bridgeless high-power-factor buck converter, IEEE Trans. Power Electron. 2011; 26(2):602-611.
19. Xie X, Zhao C, Zheng L, Liu S. An improved buck PFC converter with high power factor, IEEE Trans. Power Electron. 2013; 28(5):2277-2284.
20. Ohnuma Y, Itoh J. A novel single-phase buck PFC AC-DC converter with power decoupling capability using an active buffer, IEEE Trans. Ind. Appl. in press.
21. Zane R, Maksimovic D. Nonlinear-Carrier control for high-power-factor rectifiers based on up-down switching converters," IEEE Trans. Power Electron. 1998; 13(2):213-221.
22. Chen J, Maksimovic D, Erickson RW. Analysis and design of a low-stress buck-boost converter in universal-input PFC applications, IEEE Trans. Power Electron. 2006; 21(2):320-329.
23. ABB drives. Technical guide No. 6, Guide to harmonics with AC drives
24. Shweta Srivastava, Sanjiv Kumar. Comparative analysis of improved quality three phase ac/dc converter International Journal of Emerging Technology and Advanced Engineering. 2012; 2(9). ISSN 2250-2459.