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Design of a low Jitter PLL based on self-biased techniques

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Abstract
A self-biased PLL with fixed ratio of bandwidth to input frequency was designed in paper. The self-biased PLL had the little influence of the process, temperature and voltage. VCO was optimized to reduce the jitter. The PLL operated in the frequency range from 500MHZ to 3125MHZ with 1.2V power supply in SMIC 65nm CMOS process. Simulation results showed the PLL had a peak-to-peak jitter of 8.7ps at 1.875GHZ output frequency with 32 mW of power.

Keywords: Self-biased; PLL; VCO; Low Jitter

1. Introduction

Phase locked loop (PLL) is an important part of the chip, it can provide high frequency stability of the clock signal, widely used in communication and other fields. Designing a PLL requires the consideration of many factors with mutual constraints, such as loop bandwidth, jitter, and stability. Reducing jitter is required to increase the loop bandwidth. Maintaining the stability of the phase-locked loop is required to limit the loop bandwidth less than the minimum input frequency of 1/10 [1]. With the increase of the frequency of the PLL, the requirements of the jitter are becoming higher and higher. The traditional PLL is sensitive to the process, temperature and power, which limits the loop bandwidth of the PLL and it is difficult to obtain good jitter performance. G. Maneatis John proposed a structure of self-bias PLL, the self-bias PLL can adapt to these changes [2].

The advantage of the self-bias PLL is that the ratio of the loop bandwidth to the input frequency is fixed. The loop bandwidth can be changed with the change of the input frequency, which is equivalent to the expansion of the loop bandwidth, so the self-bias PLL has good jitter performance.

2. The Principle of Self-bias PLL

Self-bias PLL is an improvement of the traditional charge pump PLL. The structure of the traditional charge pump PLL is shown in Figure 1,which is made up of the phase detector (PFD), charge pump (CP), loop filter (LF), voltage controlled oscillator (VCO), frequency divider (DIV).

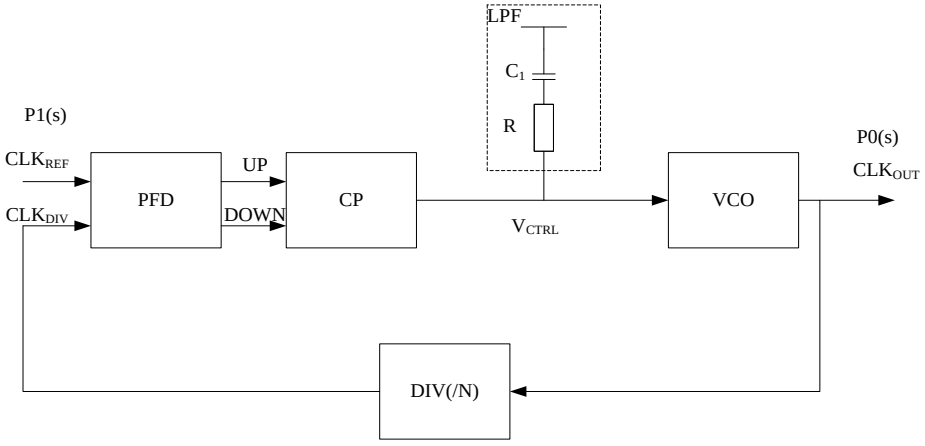

Fig 1: The Traditional Charge Pump PLL

The charge pump PLL is analyzed by the method of S domain. Assuming that the input is P1 (S), and the output is P0 (S).

$$P_0(S) = [\frac{P_1(S) - P_0(S)}{N}]\frac{I_{CP}}{2\pi}(\frac{C_1SR+1}{C_1S})\frac{K_{VCO}}{S} \quad (1)$$

In the formula, I_{CP} is the output current for CP, K_{VCO} is the gain of VCO. The closed-loop transfer function of the phase locked loop can be obtained by the formula (1).

$$H(S) = \frac{P_0(S)}{P_1(S)} = \frac{\frac{I_{CP}K_{VCO}}{2\pi}(RS+\frac{1}{C_1})}{S^2 + \frac{I_{CP}RK_{VCO}}{2\pi N}S + \frac{I_{CP}K_{VCO}}{2\pi NC_1}} \quad (2)$$

By the formula (2), we can know the bandwidth ω_N and attenuation factor ζ, the expressions are as follows.

$$\omega_N = \sqrt{\frac{I_{CP} K_{VCO}}{2\pi N C_1}} \quad (3)$$

$$\zeta = \frac{R}{2}\sqrt{\frac{I_{CP} C_1 K_{VCO}}{2\pi N}} \quad (4)$$

By the formula (3) and (4), it can be concluded that the loop bandwidth and attenuation factor are affected by K_{VCO}, I_{CP}, C1, R. Multi-parameters limit the loop bandwidth, which cannot keep the loop bandwidth at the maximum value, limiting the performance of the PLL.

The structure of self - bias PLL is shown in Figure 2.

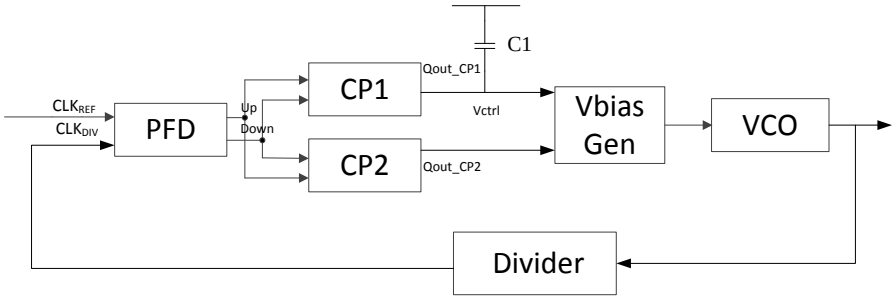

Fig 2: The Self - bias PLL

The bandwidth and attenuation factor of the self - bias PLL can be obtained by the Figure 2, and the formulas are as follows :

$$\frac{\omega_N}{\omega_{REF}} = \frac{1}{2\pi}\sqrt{xN}\sqrt{\frac{C_B}{C_1}} \quad (5)$$

$$\zeta = \frac{y}{4}\frac{1}{\sqrt{xN}}\sqrt{\frac{C_B}{C_1}} \quad (6)$$

In the formula, x is the ratio of charge pump current and the bias current of VCO, y is the ratio of equivalent load resistance of VCO and the symmetric load resistance of bias generator, x and y area fixed value. C_B is the equivalent total capacitance of bias generator. By formula (5) and (6), we can know that bandwidth and attenuation factor are only related to CB/C1 while CB/C1 can be through the layout design to a constant, so the self-biased PLL loop bandwidth can remain unchanged.

3 Main Modules of the Self-bias PLL

3.1 Phase frequency detector (PFD) and charge pump (CP)

As shown in Figure 3, the phase frequency detector is based on the classic D trigger and delay unit. The time delay unit is used to eliminate the dead zone and improves the phase discrimination accuracy. D trigger uses TSPC dynamic logic structure, the structure is simple and the working frequency is high.

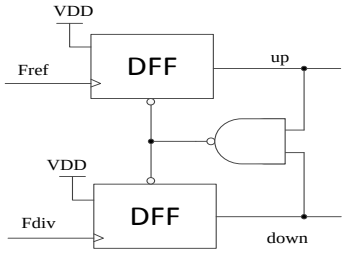

Fig 3: Phase frequency Detector (PFD)

In Figure 4, the charge pump uses the method of offset-cancelled [4].

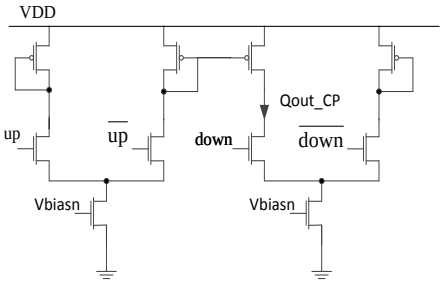

Fig 4: Charge Pump

3.2 Voltage controlled oscillator（VCO）

In this paper, the structure of ring voltage controlled oscillator is used. VCO is made up of four delay units, and the delay unit is shown in Figure 5. The time delay unit is based on the symmetrical load and the self-biasing technique. According to the viewpoint of literature [5] the good jitter performance can be obtained when the discharge constant of the output node of the delay unit is large. Therefore, the MOS tube (equivalent to a capacitor) is added between the node A and the output node, and the discharge constant of the output node becomes larger, which can obtain good jitter performance. In order to further optimize the jitter performance, the 4 delay elements are connected to the node A, which can reduce the impact of power supply noise and reduce the jitter.

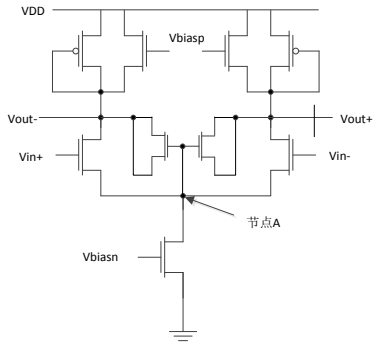

Fig 5: Delay Unit of VCO

4 Layout Design and Simulation Results

The design of PLL uses SMIC65nm technology, the overall layout as shown in Figure 6.

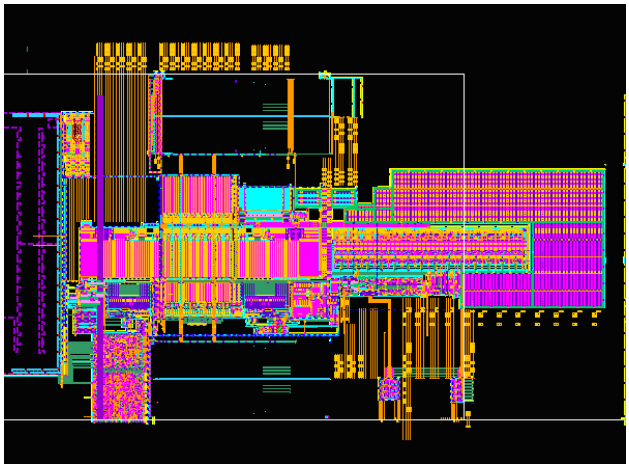

Fig 6: the layout of PLL

Phase locked loop works in the 1.2V supply voltage; the output frequency is 500M ~ 3.125GHZ. Through the Finesim simulation tool for the simulation of the phase locked loop. The results areas shown in Figure 7, when the input frequency is 312.5MHZ, the output frequency of PLL is expanded to 3.125GHZ.

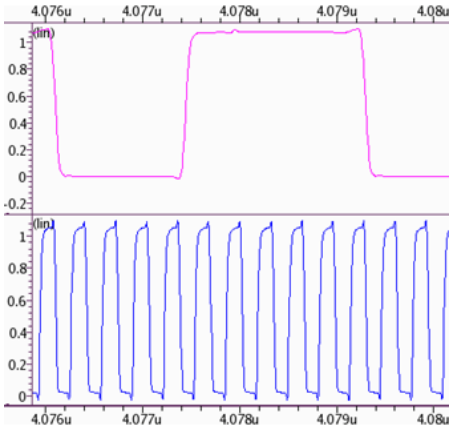

Fig 7: the result of output

Figure 8 is the output eye diagram when output frequency is 1.875GHZ without the improved VCO; the peak-to-peak jitter is 10.3ps. Figure 9 is the output eye diagram when output frequency is 1.875GHZ with the improved VCO; the peak-to-peak jitter is 8.7ps. By comparing the simulation results, we can find that the improvement of VCO can reduce the jitter.

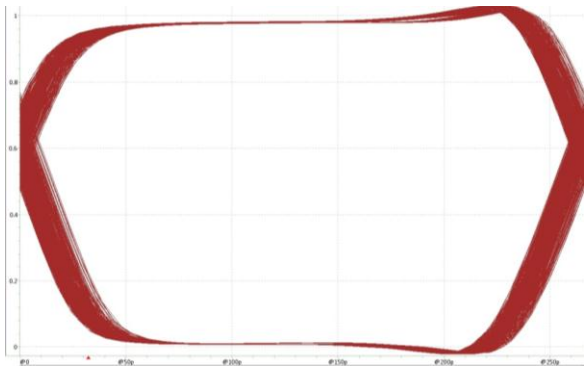

Fig 8: the output eye diagram without the improved VCO

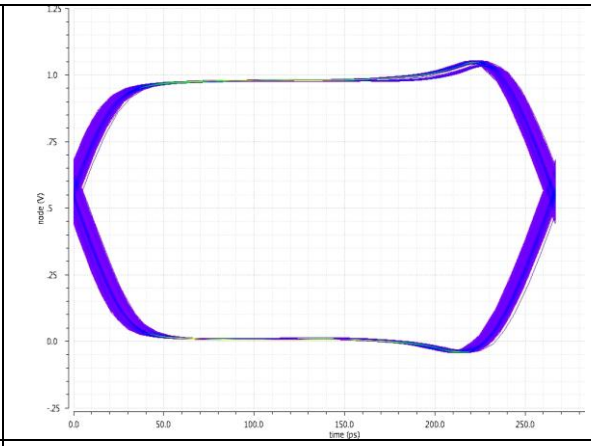

Fig 9: the output eye diagram with the improved VCO

In Table 1, compared with the self-bias PLL published in the reference literature 6. The jitter is smaller, which shows that the design has good jitter performance.

Table 1: Performance comparison of PLLs

PLL	This paper	The reference literature 6
manufacturing process/um	0.065	0.13
Output frequency/MHZ	500-3125	25-2400
supply voltage/V	1.2	1.2
Peak-to-peak Jitter/ps	8.7（1.875GHZ）	21.34(1.36GHZ)
Core power consumption/mw	32	8.4-16.8

5 Conclusion

In this paper, a kind of self-bias PLL is designed based on the SMIC65nm process, and the output frequency is 500M-3125MHZ. The VCO delay unit is improved, and the simulation results show that the PLL has good jitter performance.

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