

Power factor corrected Buck – boost converter fed BLDC motor drive

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Abstract

This paper present about the design of a power factor corrected bridgeless Buck- boost converter fed Brushless motor drive. The Brushless DC motor (BLDC) is used as a solution for a cost effective and low power motor drive. By controlling the DC link voltage of the BLDC motor drive, the speed of the drive is adjusted. The voltage source inverter (VSI) is fed by this DC link voltage. This makes the VSI to operate at fundamental frequency switching which utilizes the electronic commutation of BLDC motor. The bridgeless configuration of the Buck-boost is used to eliminate the switching losses related with the diode bridge rectifier and is operating in the discontinuous inductor current mode, so that it provides an inherent PFC at AC mains. In this paper by varying the supply voltage and wide range of speed control, performance of the drive is analyzed. The steady state and dynamic analysis of the system is performed in MATLAB/SIMULINK environment.

Keywords: Power factor, Buck-boost, Brushless DC motor (BLDC), voltage source inverter (VSI)

1. Introduction

The application of BLDC in home appliances such as fan, water pumps, blowers, actuators in advance aircraft and satellite system, phonograms and tape drives etc. is due to the higher efficiency, flexibility, long life, low electro-magnetic interference problem.

A BLDC motor has a construction which is similar to that of a synchronous motor with permanent magnet rotor. The stator has usually a convention three phase ac winding which is either star or delta connected. There are two types motor based on the positioning of permanent magnet. If the permanent magnets (PM) are on the surface of the rotor, it is called as surface mounted PM rotor. If the magnets are placed on grooves, they are called as interior PM rotor. The difference between PM synchronous motor and BLDC motor is the way of excitation of it is stator. In PM synchronous motor, the phase windings are connected to a three phase supply of line frequency which in produce a smoothly rotating stator mmf revolving at the speed given by f/p mechanical revolutions per second. In a BLDC motor, the stator windings are sequentially switched with dc current or voltage through a three phase inverter. The switching pattern and the frequency are controlled by the rotor position and speed.

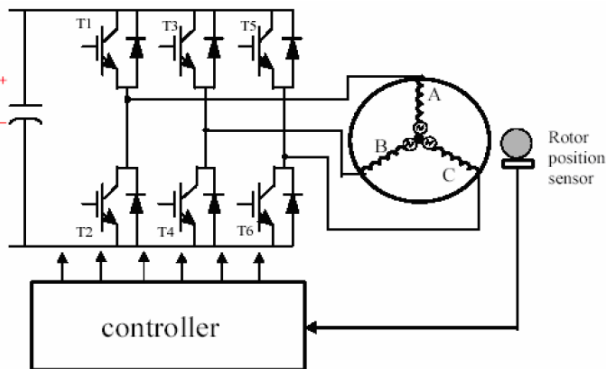


Fig 1: Basic configuration of BLDC motor

The electronic commutation is used here so the BLDC motor can be referred to as an electronically commuted motor. Each commutation sequence has one of the winding energized to positive power and the second winding energized to negative power and the third winding is non- energized. Torque is produced by the interaction of magnetic field produced by the stator windings and the permanent motor.

The problems related to power quality need quite attention now a days. The THD will be in order of 65% when the BLDC is fed by a diode bridge rectifier. So for improving the power quality at the ac mains BLDC fed by diode bridge rectifier (DBR) along with a power factor corrected converter is used. The mode of operation of the converter also need quite attention. It can be either continuous conduction mode (CCM) or discontinuous conduction mode (DCM). In CCM the current through the inductor is a constant, while in DCIM current is discontinuous. The DCM is preferred for the low power application, since it needs to sense only the DC link voltage. But in the CCM it needs to sense the source current also. So they need to two sensors.

The PWM scheme for the VSI is used for the speed control which offers higher switching losses, where the losses are increased as the square of the frequency. So we are adopting a technique to vary the DC link voltage for the speed control. This will helps to reduce the switching losses and enables the VSI to operate in the fundamental switching frequency. In order to improve the efficiency and to obtain the power quality standards, power factor correction is done by using a Buck-Boost converter. The buck boost converter is selected after a comparative study on various type of converter topologies.

2. Proposed BLDC motor drive

The figure above shows the block diagram of the proposed system. Here the buck boost converter works in DCIM. From the ac mains, the LC filter is used for shaping the waveform. This is given to the input of the power factor correction converter. The dc link voltage from the converter is given to the voltage source inverter. By varying the dc link voltage the

speed can be adjusted. Electronic commutation of the motor is done with the help of control circuit which utilizes the rotor position obtained using hall-effect sensor. Switching of the buck boost converter is also obtained from the control unit. That is the pulses for the switch in the Buck boost converter is obtained from the PWM generator. The process taking place in the control unit is as follows; using a reference speed a

reference voltage is producing. This voltage is compared with the dc link voltage and produces an error voltage, which is given to a PI controller. This voltage waveform and the saw tooth waveform are compared in the PWM generator and produces the pulses for switching in the buck boost converter. In order to study about the drive at a practical supply condition, the supply voltage is varied.

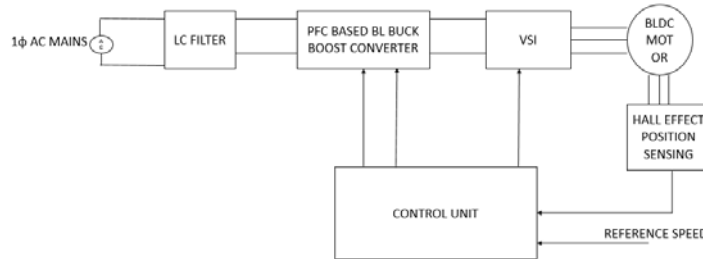


Fig 2: Proposed BLDC motor drive

3. Operation of the buck boost converter

The operation is classified into two parts as, the operation during positive and negative half cycles and the operation during a complete cycle.

3.1 Operation during positive and negative cycle

The switches Sw1 and Sw2 operated for the positive and negative half cycle. Here the inductor current becomes discontinuous for certain time. Figure below shows the operation during the positive half cycle.

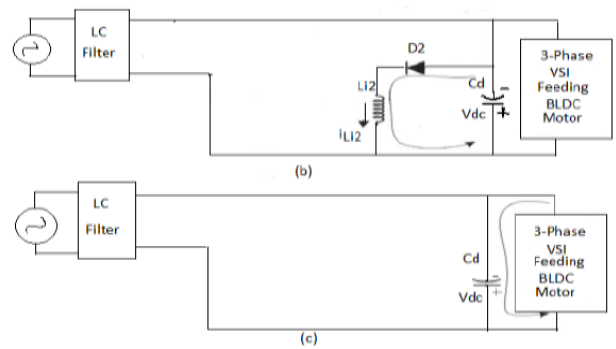


Fig 4: Working during negative half cycle

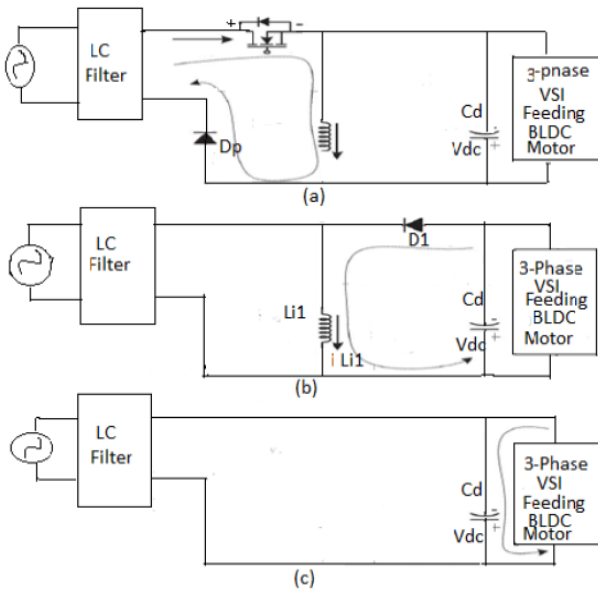
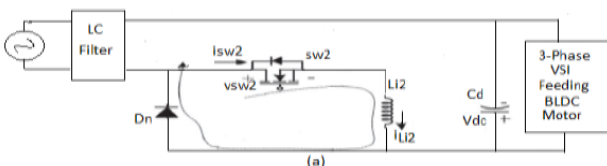


Fig 3: Working during the positive half cycle.

3.2 Operation during complete switching cycle

Working during the negative half cycle is shown below,



During complete switching, there are three modes of operation

In mode 1, the Sw1 conducts to charge the inductor Li1. The circuit completes through the Li1 and Dp. But the DC link capacitor gets discharged as shown in figure below.

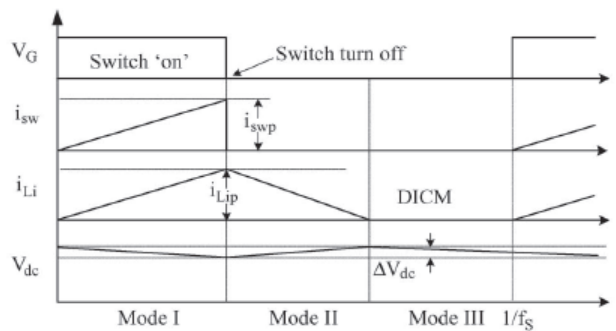


Fig 5: Waveform during complete cycle.

In mode 2, the Sw1 is off and the energy stored in the inductor is transferred to the dc link capacitor. This is shown in figure 3(b). So the current in the inductor reaches to zero as shown in the figure 5.

In mode 3, none of the switches or the diodes are in conducting mode. The energy in the inductor is completely transferred and there is no current after that. The load is supplied by the dc link voltage. The whole operation repeats when the Sw1 turned on.

4. Design of the proposed drive

PFC BL buck–boost converter was created to operate in DICM the current in inductors L_{i1} and L_{i2} becomes discontinuous in a switching period. For a BLDC of power rating 251 W, a power converter of 350 W (P_o) is designed. For a supply voltage by having an rms value of 220 V, the average voltage appearing at the input side can be calculated as follows,

$$V_{in} = 2\sqrt{2}V_s / \pi = 2\sqrt{2} \times 220 / \pi \approx 198 \text{ V} \quad \dots 4.1$$

The relation governing the voltage conversion ratio for a buck–boost converter is given as

$$d = V_{dc} / (V_{dc} + V_{in}) \quad \dots 4.2$$

The proposed converter is designed in such a way that dc link voltage control from 50 V ($V_{dc \text{ min}}$) to 200 V ($V_{dc \text{ max}}$) with a nominal value ($V_{dc \text{ des}}$) of 100 V. So the value of d for $V_{dc \text{ max}}$ and $V_{dc \text{ min}}$ are 0.2016 and 0.5025.

4.1 Design of Input Inductors (L_{i1} and L_{i2})

The value of inductance L_{ic1} , to work in critical conduction mode in the buck–boost converter, is given as;

$$L_{ic1} = (1-d)^2 \frac{V_{dc}}{2f_s} \quad \dots 4.3$$

R is the equivalent load resistance

D is the duty ratio

f_s is the switching frequency.

The value of L_{ic1} is calculated for minimum duty ratio d_{min} . At minimum duty ratio, the BLDC motor operating at 50 V ($V_{dc \text{ min}}$), the ability (P_{min}) is given as 90 W (i.e., for constant torque, force power is proportional to speed). So the value of $L_{ic \text{ min}}$ can be calculated as,

$$\begin{aligned} L_{ic \text{ min}} &= V_{dc \text{ min}}^2 (1 - d_{\text{min}})^2 / (P_{\text{min}} 2f_s) \\ &= 50^2 (1 - 0.2016)^2 / 90 \times 2 \times 2000 \\ &= 442.67 \mu\text{H} \quad \dots 4.4 \end{aligned}$$

The values of L_{i1} and L_{i2} are taken as less than 1/10 th of the minimum critical inductance value. Hence for the convenience the values are taken as around 35 μH .

4.2 Design of DC Link Capacitor (C_d)

The design of the dc link capacitor depend on the total amount of the second-order harmonic (lowest) current flowing in the capacitor and is derived as follows.

For the PFC operation, the supply current (i_s) is in phase with the supply voltage (v_s). Hence, the input power,

$$\begin{aligned} P_{in} &= \sqrt{2}V_s \sin\omega t \times \sqrt{2}I_s \sin\omega t \\ &= V_s I_s (1 - \cos 2\omega t) \quad \dots 4.5 \end{aligned}$$

The second term in this equation corresponds to the second order harmonics. There for the value of dc link capacitor is obtained as

$$i_c(t) = V_s I_s \cos 2\omega t / V_{dc} \quad \dots 4.6$$

Voltage ripple corresponding to this current

$$\Delta V_{dc} = 1/C_d \int i_c(t) dt$$

$$= I_d \sin 2\omega t / 2\omega C \quad \dots 4.7$$

The value of C_d is obtained as,

$$C_d = I_d / 2\omega \Delta V_{dc} \quad \dots 4.8$$

$$\begin{aligned} &= (P_o / V_{dc \text{ des}}) / (2\omega \Delta V_{dc}) \\ &= (350 / 100) / (3 \times 3.14 \times 0.03 \times 100) = 1857.7 \mu\text{F} \quad \dots 4.9 \end{aligned}$$

4.3 Design of Input Filter (L_f and C_f)

An LC filter of second order is used at the input side in order to absorb the harmonics. The maximum value of filter capacitance is given as

$$\begin{aligned} C_{\text{max}} &= I_{\text{peak}} \tan(\theta) / \omega_L V_{\text{peak}} \quad \dots 4.10 \\ &= (350 / 220) \tan(1) / (314 \times 220 \sqrt{2}) \\ &= 401.98 \text{ nF} \end{aligned}$$

I_{peak} , V_{peak} , ωL , θ represents peak value of supply current, supply voltage, line frequency and displacement angle. Hence, a benefit of C_f is taken as 330 nF.

The value of the filter inductor is created by considering the origin impedance (L_s) of 4%–5% of the bottom impedance. Hence, the excess value of inductance required is given as

$$\begin{aligned} L_f &= L_{\text{req}} + L_s \\ &= L_{\text{req}} + 0.04 (1/\omega L) (V_s^2 / P_o) \quad \dots 4.11 \end{aligned}$$

$$\begin{aligned} L_{\text{req}} &= 1 / (4 \times 10^{-2} \times 2000^2 \times 330 \times 10^{-9}) - 0.04 (1/314) (220^2 / 350) \\ &= 1.57 \text{ mH} \quad \dots 4.12 \end{aligned}$$

$$f_L < f_c < f_{\text{sw}} \quad \dots 4.13$$

f_c is the cut off frequency. Hence, a value of f_c is taken as $f_{\text{sw}}/10$. A low-pass filter with inductor and capacitor of 1.6 mH and 330 nF is selected for this particular application.

5. Control of PFC circuit and BLDCM

5.1 Control of PFC converter

The controlling of the PFC converter is done with the help of creating pulses for the switches. Pulses are created by comparing the DC link voltage and a reference voltage. The reference voltage is produced by multiplying the reference speed with a constant (K_v).

$$V_{dc}^* = K_v \omega^* \quad \dots 4.14$$

The error signal produced is

$$V_e(k) = V_{dc}^*(k) - V_{dc}(k) \quad \dots 4.15$$

Here k represents the sampling time. This error voltage is given to a PI controller. The output of the voltage controller is compared with the high frequency saw tooth signal (m_d) to generate PWM pulses for the switches.

$$\text{For } v_s > 0; \quad \left\{ \begin{array}{l} \text{if } m_d < V_{cc} \text{ then } S_{w1} = \text{'ON'} \\ \text{if } m_d \geq V_{cc} \text{ then } S_{w1} = \text{'OFF'} \end{array} \right\}$$

$$\text{For } v_s < 0; \quad \left\{ \begin{array}{l} \text{if } m_d < V_{cc} \text{ then } S_{w2} = \text{'ON'} \\ \text{if } m_d \geq V_{cc} \text{ then } S_{w2} = \text{'OFF'} \end{array} \right\} \quad \dots 4.16$$

5.2 Control of BLDCM

The BLDCM is controlled by proper switching of the VSI according to the output occurred from the hall- effect sensor. The switching pattern for the VSI is given below

Table 1: Switching states for VSI of BLDC motor

Θ (degrees)	Hall signals			Switching states					
	H _a	H _b	H _c	S ₁	S ₂	S ₃	S ₄	S ₅	S ₆
NA	0	0	0	0	0	0	0	0	0
0-60	0	0	1	1	0	0	0	0	1
60-120	0	1	0	0	1	1	0	0	0
120-180	0	1	1	0	0	1	0	0	1
180-240	1	0	0	0	0	0	1	1	0
240-300	1	0	1	1	0	0	1	0	0
300-360	1	1	0	0	1	0	0	1	0
NA	1	1	1	0	0	0	0	0	0

6. Performance of simulated proposed drive

The proposed design for the BLDC motor is simulated in the MATLAB/ Simulink environment. The performance of the drive is evaluated by the speed control and the supply voltage variation. The parameter associated with the BLDCM such as torque. Stator current, speed are analyzed. The source voltage and source voltage are also analyzed. The power factor of the system is also analyzed for different voltage and speed conditions. The simulation diagram is as shown.

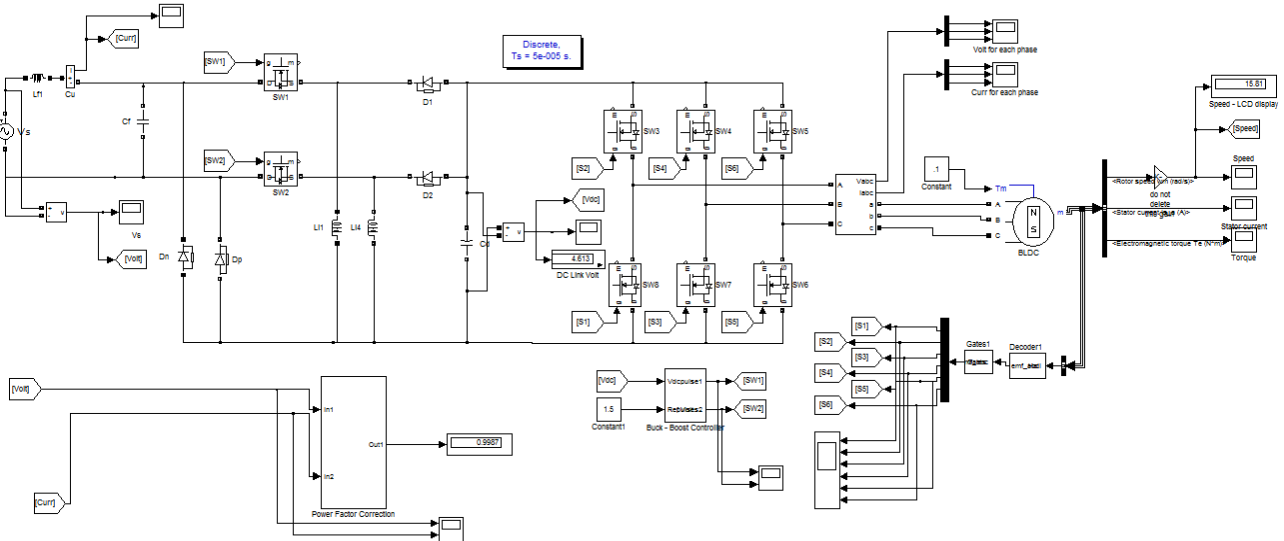
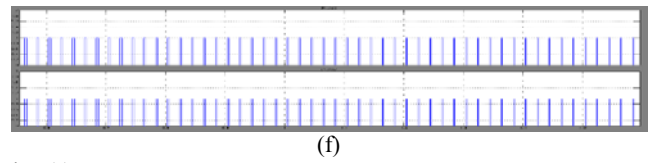
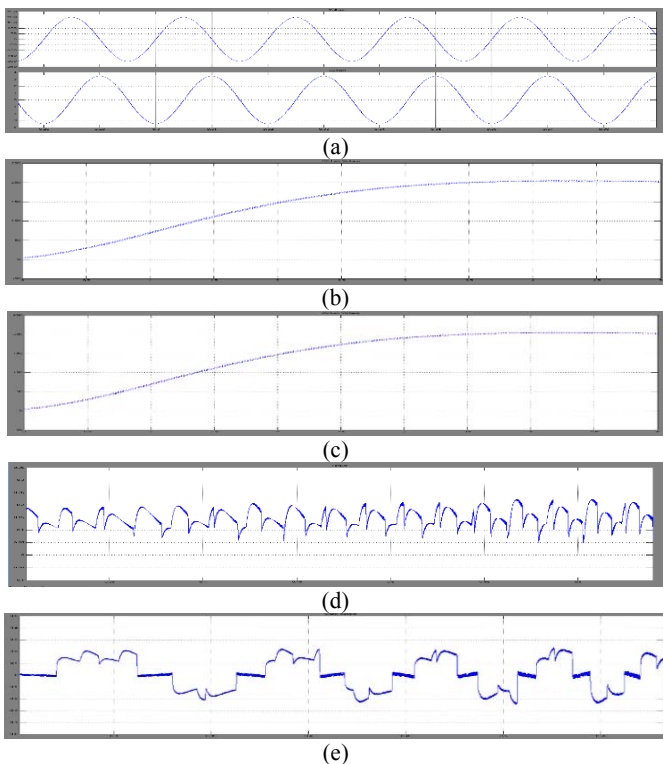


Fig 6: Simulation diagram of proposed drive

6.1 Steady state performance

The steady state analysis of the proposed drive for rated condition of 200 Vis shown in figure below.



Time(s).....>

Fig 7: Steady state performance of the drive (a) source voltage and current, (b) dc link voltage, (c) speed in RPM, (d) electromagnetic torque in Nm, (f) switching pulses for Sw1 and Sw1

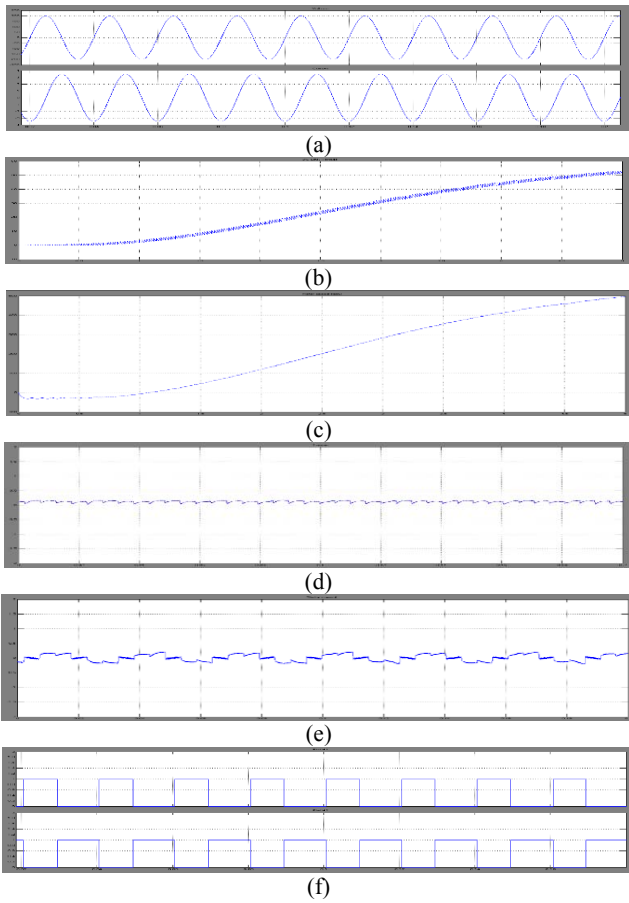
The graphs shows the proper working of the BLDC motor and the Buck boost converter at the rated dc link voltage. The performance of the drive at speed control by varying the dc link voltage from 50 to 200V are shown in the table below.

Table 2: Performance of the drive under varying dc link voltage

V _{Dc} (V)	PFC	Speed (RPM)
50	0.9998	492
65	0.9999	644
83	0.9999	818
108	0.9999	993
112	0.9999	1103
130	0.9999	1294
143	0.9999	1417
154	0.9999	1521
188	0.9999	1840
195	0.9999	1926
200	0.9999	1975

6.2 Dynamic performance

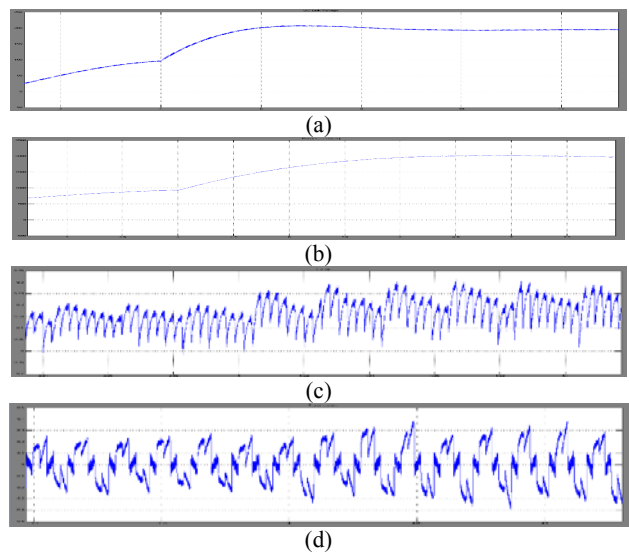
The dynamic performance of the system during starting 50V



Time (s).....>

Fig 8: Dynamic performance during starting drive (a) source voltage and current, (b) dc link voltage, (c) speed in RPM, (d) electromagnetic torque in Nm, (f) switching pulses for Sw1 and Sw2

The performance under dc link voltage variation from 100V to 200V



Time(s).....>

Fig 9: Dynamic performance during speed control (a) dc link voltage, (b) speed (c) torque (d) stator current

6.3 Performance under supply voltage variation

The performance of the drive is also evaluated for supply voltage variation. It varies from 150V to 250V. It's analyzed that the power quality indices are within the specified limit.

Table 3: Performance of the drive under supply voltage variation

Vs(V)	THD (%)	PF
150	0.02	0.998
170	0.03	0.998
200	0.03	0.999
230	0.03	0.999
250	0.03	0.999

7. Conclusion

A PFC BL buck–boost converter-based VSI-fed BLDC motor drive has been proposed targeting low-power applications. The DC link voltage is controlled to obtain the speed control and the VSI is made to operate at the fundamental frequency. The power factor correction is obtained at the front end by using the Buck boost converter. The drive performance is analyzed for various conditions such as variable supply voltage and the DC link voltage. In both the cases desired performance is obtained. The power quality indices such as THD and PF are within the acceptable limits in both the cases.

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