International Journal of Multidisciplinary Research and Development

IJMRD 2015; 2(4): 93-96
www.allsubjectjournal.com
Received: 12-03-2015
Accepted: 29-03-2015
e-ISSN: 2349-4182
p-ISSN: 2349-5979
Impact Factor: 3.762

D. B. Rane
Department of Electronics
Engg Pravara Rural
Engineering College, Loni

Srivastava Vinay Pratap
Department of Electronics
Engg Pravara Rural
Engineering College, Loni

Sinha Sucheta Dipankar
Department of Electronics
Engg Pravara Rural
Engineering College, Loni

Singh Sachin Arvind
Department of Electronics
Engg Pravara Rural
Engineering College, Loni

Correspondence:
Sinha Sucheta Dipankar
Department of Electronics
Engg Pravara Rural
Engineering College, Loni

FPGA based high speed, low power 32 bit*32 bit multiplier

D. B. Rane, Srivastava Vinay Pratap, Sinha Sucheta Dipankar, Singh Sachin Arvind

Abstract
In the proposed paper, a mixed number representation is being used in order to develop a low power, high speed multiplication algorithm. The redundant binary (RB) adder and booth decoder along with sign magnitude notation of the multiplicand, helps in achieving the reduced switching activity and low power dissipation. The high speed operation is achieved by accumulation of partial products (PP) through carry propagation free (CPF) using RB notation. Due to this, the switching activity during the PP generation process can be reduced on an average by 90%.The design proposed in paper dissipates much less power comparatively and is 18% faster on an average.

Keywords: Less power consuming multiplication algorithm, VLSI architecture, Xilinx Spartan-3A FPGA.

1. Introduction
Multiplication is a fundamental operation in most signal processing algorithms. Multipliers have large area and consume considerable power. Therefore, less power consuming multiplier design has been an important and requirement in low power VLSI system design. Fast multipliers are essential parts of digital system processing systems. The speed of multiplier operation is of great importance in digital signal processing as well as in the general purpose processors today. The basic multiplication principle is in two fold i.e. evaluation of partial products and accumulation of shifted partial products. In fact 8.72% of all instructions in a typical scientific program are multiplies. In typical processes, multiplication takes between two and eight cycles. Consequently, having high-speed multipliers is critical for the performance of processors.
Processor designers have recognized this and have devoted considerable silicon area for the design of multipliers. Recent advances in integrated circuit fabrication technology have resulted in both smaller feature sizes and increased areas. Together, these factors have provided the processor designer the ability to fully implement high-speed multipliers. Here, the expected switching activity and power dissipation can be reduced by using SM notation for the multiplicand; two's complement representation of the multiplier and the use of RB representation for the PP accumulation. In order to generate the PPs, the negation of the multiplicand is required and the ESA is reduced during that time. High speed operation is maintained with the help of the RB notations that are being used for the accumulation of the PPs. The CPF addition is being executed by the redundant binary numbers. It is essential to notice the fact that the proposed algorithm and the VLSI architecture is more complex in terms of the number conversion but the advantage of it is that it happens to be more energy efficient and has a faster operating speed.

2. Less power generation:
The expected switching activity and power dissipation can be reduced by using SM notation for the multiplicand; two's complement representation of the multiplier and the use of RB representation for the PP accumulation. In order to generate the PPs, the negation of the multiplicand is required and the ESA is reduced during that time. High speed operation is maintained with the help of the RB notations that are being used for the accumulation of the PPs. The CPF addition is being executed by the redundant binary numbers. It is essential to notice the fact that the proposed algorithm and the VLSI architecture is more complex in terms of the number conversion but the advantage of it is that it happens to be more energy efficient and has a faster operating speed.

3. High Speed Generation:

Multiplication of two binary fractions is normally implemented as the addition of number of summands, each simple multiplicand, chosen from a limited set of multiplies on the basis of one or more multiplier digits. Acceleration of the process is based on the following factors:

1) Reduction in the number of summands.
2) Acceleration in the formation of summands.
3) Acceleration in the addition of summands.

4. Booth Multiplier:

Booth multiplier can be used in different modes such as **radix-2, radix-4, radix-8** etc. But we decided to use **Radix-2 Booth's Algorithm.** Booth algorithm provides a procedure for multiplying binary integers in signed-2's complement representation. According to the multiplication procedure, strings of 0's in the multiplier require no addition but just shifting and a string of 1's in the multiplier from bit weight 2k to weight 2m can be treated as 2k+1 - 2m. Booth algorithm involves recoding the multiplier first. In the recoded format, each bit in the multiplier can take any of the three values: 0, 1 and -1.Suppose we want to multiply a number by 01110 (in decimal 14). This number can be considered as the difference between 10000 (in decimal 16) and 00010 (in decimal 2). The multiplication by 01110 can be achieved by summing up the following products:

- 24 times the multiplicand (24 = 16)
- 2's complement of 21 times the multiplicand (21 = 2).

In a standard multiplication, three additions are required due to the string of three 1's.This can be replaced by one addition and one subtraction. The above requirement is identified by recoding of the multiplier 01110 using the following rules summarized in table.

Q_n	Q_{n+1}	Recoded bits	Operation performed
0	0	0	Shift
0	1	+1	Add M
1	0	-1	Subtract M
1	1	0	Shift

Fig: 4.1

5. Architecture:

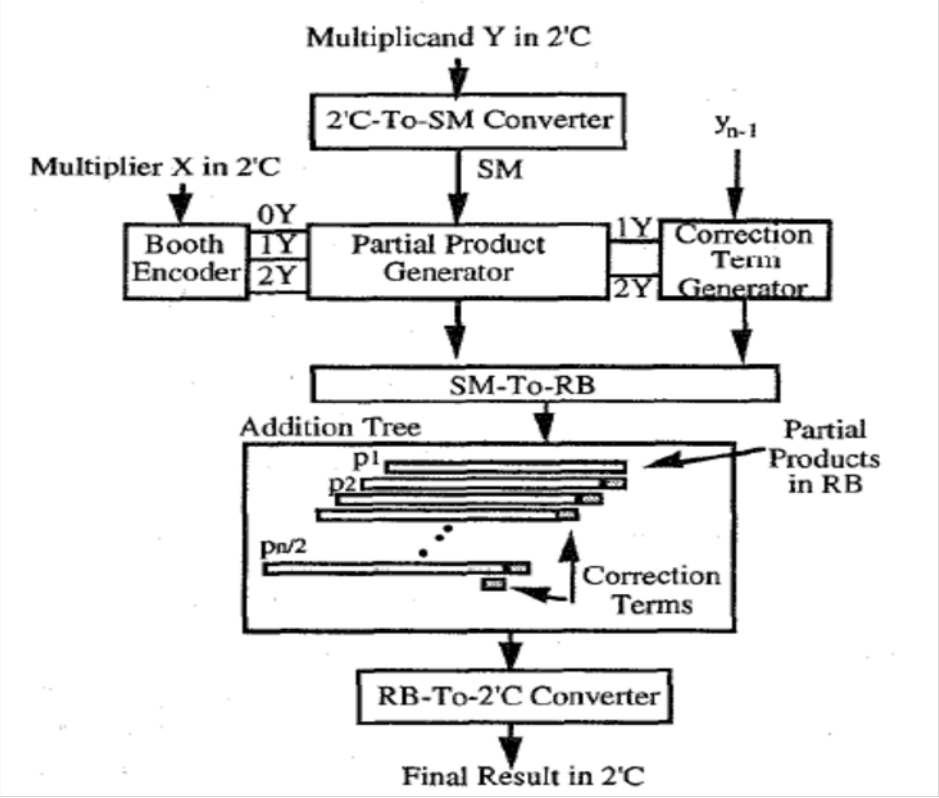

Fig: 5.2

The arithmetic operations can be easily carried out with 2'C numbers and the Booth's algorithm can largely reduce the number of PPs. But, the Booth's algorithm often requires the negation of the multiplicand, and the negation of a 2'C number requires many bits to be switched which results in high switching activity. Without losing generality, we use the radix-4 Booth's algorithm to demonstrate the probability of the negation of the multiplicand to be generated and how many bits on average have to be switched. This would give us the **Expected Switching Activity (ESA)**, during the PP Generation.

5. Block Diagram:

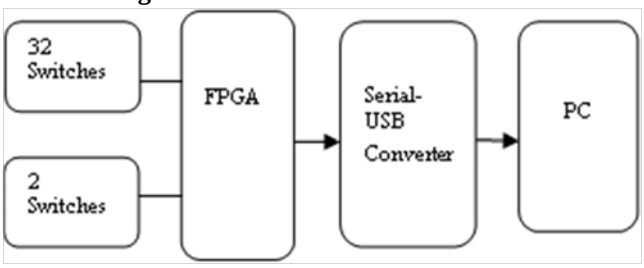

Fig: 5.1

Here we will give input of 32 bit multiplier by the help of 32 switches module, and for selection of the two multipliers are selected by the 2 switches module. As the input is feed to the FPGA, the FPGA will multiply the two input data and the result will be displayed on personal computer with the help of serial to USB converter.

6. Multipliers in FPGA:

FPGA have a number of features to fortify the chips arithmetic capabilities. Carry logic and dedicated routing continues to provided in past generations. Dedicated AND gates accelerate array multiplication operations. Most significant addition is the dedicated 32*32 two's complement multiplier block. With these dedicated multipliers in each device, fast arithmetic functions can be implemented with minimal use of the general purpose resources. In addition to the performance advantage, dedicated multiplier requires less power than CLB based multiplier. The multiplier blocks share routing resources with block selected RAM memory, allowing for increased efficiency for many applications. Cascading of multiplier can be implemented with additional logic resources in local Spartan 3 slices. Application such as signed – signed, signed – unsigned, unsigned – unsigned multiplication, logical, arithmetic and others are easily implemented. FPGAs can be characterized by the following items:

- High production cost
- Low design density
- Programmable fabric adds significant overhead
- No NRE and Re-Spin cost
- Low development effort
- Low dead-time
- simplified timing
- No test vectors
- Relaxed verification
- Physical design is "hands-off

The FPGA board that we are using is an Elbert V2 which is an easy to use development board featuring Xilinx Spartan-3A FPGA. Elbert V2 is specially designed for experimenting and learning system design with FPGAs. This development board features Xilinx XC3S50A TQG144 FPGA. The USB 2.0 interface provides fast and easy configuration download to the on-board SPI flash. You don't need a programmer or special downloader cable to download the bit stream to the board.

7. Algorithm:

Step 1: We will be using the multiplicand in SM notation and keep the multiplier in 2'C form.

Step 2: Generate all the PPs shown in SM notation by applying booth algorithm.

Step 3: The Partial products in SM notation is converted into SM representation.

Step 4: Summing all the PPs by a RB adder.

Step 5: Convert the final result from RB notation into 2'C notation.

The corresponding VLSI architecture for the algorithm composed of two major parts: the PP generator and the redundant binary addition tree. The key components in this architecture are: the RB adder in the addition tree and the Booth decoder in the FF generator. A novel design for the RB adder and Booth decoder based on SM coding has been developed. The new RB adder has a critical path delay of 4 gate-delays, while the previously reported fastest RI3 adder has a critical path delay of 5 gate-delays. The new Booth decoder needs only 3 transistors and 3 control lines instead of 9 transistors and 5 control lines for the 2'C based booth decoder.

8. Flowchart:

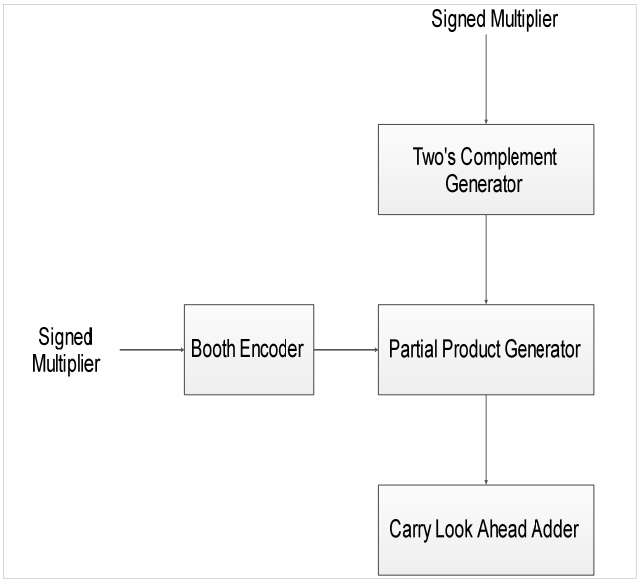

Fig: 8.1

9. Merits:

- Multiplier performs at higher speed.
- Less delay in processing of the system.
- The proposed design dissipates much less power and is 18% faster on average.
- Low power consumption.
- By implementing this project of Xilinx FPGA we will be able to implement different DSP related applications

10. Applications:

- Multiplier.
- High speed processors.
- DSP (Digital Signal Processors).
- DWT
- Radar communications.
- Wherever mathematical calculations (multiplication) are required.

11. Conclusion:

A low power multiplication algorithm and its VLSI architecture are proposed. The reduced switching activity and low power dissipation are achieved through the SM representation for the multiplicand and through a novel design of the RB adder and the Booth decoder for the SM numbers. The high speed operation is achieved through the CFF accumulation of the FPs by using RB numbers. The SM-to-RB conversion is carried out by grouping the sign bit with all other bits, which does not require any operation except some wiring. Analytical study indicates that the ESA in the multiplicand negation process for PP generation can be reduced on average by 90 percent. Further research on the low power redundant binary addition tree design is under investigation.

Reference:

1. C.Wallace, "A Suggestion for a Fast Multiplier," IEEE Trans. on Electronic Computer, Vol.EC- 13, pp. 14- 17, February 1964.
2. Menghui Zheng and Alexander Albicki "Low Power and High Speed Multiplication Design

Through Mixed Number Representations" Institute of Electrical and Electronics Engineering, Department of Electrical Engineering, University of Rochester, NY 14627, USA, 1995
3. Nishat Bano" VLSI Design of Low Power Booth Multiplier" International Journal of Scientific & Engineering Research, Volume 3, Issue 2, February - 2012
4. Pouya Asadi and Keivan Navi "A New Low Power 32×32-bit Multiplier" World Applied Sciences Journal 2: 341-347, 2007, ISSN 1818-4952 © IDOSI Publications, 2007
5. Partha Sarathi Mohanty "design and implementation of faster and low power multipliers" Department Of Electronics and Communication Engineering National Institute of Technology Rourkela 2009
6. Sri Ramya P, Suhali Afroz MD "VLSI implementation of 32 bit unsigned multiplier using an efficient CLAA and CSLA" IPASJ International Journal of Electronics & Communication (IIJEC) Volume 2, Issue 7, July 2014
7. H. S. Krishna prasad Puttam, P. Siva durga Rao & N. V. G. Prasad "Implementation of low power and high speed multiplier-accumulator using SPST adder and Verilog" International Journal of Modern Engineering Research (IJMER) Vol. 2, Issue. 5, Sep.-Oct. 2012

Prof. D. B. Rane obtained M.E.(Digital Electronics) from Amravati University, B.E. (Electronics Engg.) from Dr. Babasaheb Ambedkar Marathwada University, Aurangabad. He has been engaged in teaching for period of 10 years. Presently He is working as Head of Dept, Electronics Engineering at Pravara Rural Engineering College, Loni.

Mr. Vinay P. Srivastav currently pursuing the B.E. degree in Electronic Engineering from Pravara Rural Engineering College, Loni.

Ms. Sucheta D. Sinha currently pursuing the B.E. degree in Electronic Engineering from Pravara Rural Engineering College, Loni.

Mr. Sachin A. Singh currently pursuing the B.E. degree in Electronic Engineering from Pravara Rural Engineering College, Loni.