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Vehicle identification and authentication system

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Abstract
In this paper a Vehicle Identification and Authentication System is developed for traffic monitoring. To prevent unauthorized vehicles from entering the private areas, vehicle based authentication technologies are employed. The captured color image of the vehicle is converted to gray scale image. Gray scale image is converted into binary image using Sliding Concentric Windows (SCW) method. Pixels are labelled into components based on pixel connectivity using Connected Component Analysis (CCA) technique. The labelled components are examined and detected license plate is processed to isolate characters. These characters are sent to Probabilistic Neural Network (PNN). PNN uses a supervised training set to develop distributed functions within a pattern layer. Vehicle entering an area is considered as authenticated if it is registered. Registered vehicles' number plate indicates the state and district to which particular vehicle belongs to. Vehicles are considered to be authenticated, if it belongs to a particular state and district, after which the vehicles' type and other details are extracted from the database.

Keywords: Two Zigbee transceiver, LPC2148 (ARM7) microcontroller, LCD, Keypad, MAX 232, PC, Serial communication interfaces,Multiple UARTS, Power supply.

1. Introduction

In our proposed system we are using two XBEE Transceiver based embedded system based on ARM microcontroller. One system is installed inside the vehicle and other system is installed at the entrance. When the vehicle enter at the entrance it was identified by the XBEE Transceiver installed system at the gate asks driver to enter password. This password is also verified by the system at the at the gate by verifying code of the vehicle XBEE transceiver. Then the XBEE based entrance gate. Once both the vehicle identification and the driver authentication has done then the system send the information to the security guard at the gate. According to this information the guard allows or denies access to the vehicle inside the premises.

1.1 Methodology: Three type of methodology we are using:-

- Software: Embedded C and visual basic.
- Tools: keil, Flash magic.
- Target device: LPC2148 (ARM7) microcontroller.

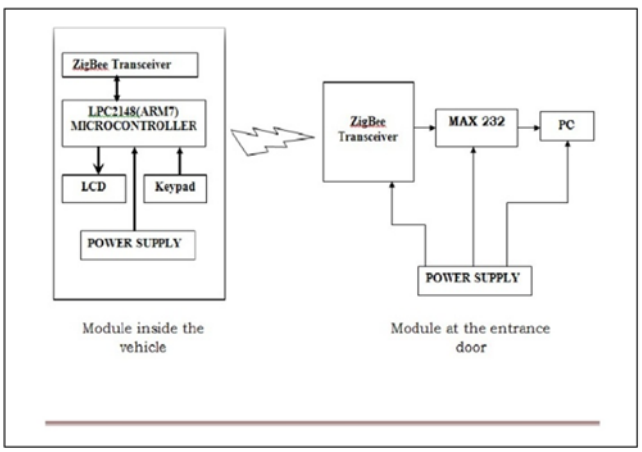

Fig 1: Block diagram of kit

2. Hardware Description

Ranging from 32 KB to 512 KB, A 128-bit wide memory interface and a unique accelerator architecture enable 32-bit code execution at the maximum clock rate. For critical code size applications, the alternative 16-bit Thumb mode reduces code by more than 30 % with minimal performance penalty. Due to their tiny size and low power consumption, LPC2141/42/44/46/48 are ideal for applications where minia turization is a key requirement, such as access control and point-of-sale. Serial communications interfaces ranging from a USB 2.0 Full-speed device, multiple UARTS, SPI, SSP to I2C-bus and on chip S RAM of 8 KB up to 40 KB, make these devic es very well 2.1 LPC2148 MICROCONTROLLER

2.1. General description

The LPC2141/42/44/46/48 microcontrollers are based on a 16-bit/32-bit ARM7TDMI-SCPU with real-time emulation and embedded trace support, that combine microcontroller with embedded high-speed flash memory suited for communication gateways and protocol converters, soft modems, voice recognition and low end imaging, providing both large buffer size and high processing power. Various 32-bit timers, single or dual 10-bit ADC(s), 10-bit DAC, PWM channels and 45 fast GPIO lines with up to nine edge or level sensitive external interrupt pins make these microcontrollers suitable for industrial control and medical systems.

2.2. Features

- 16-bit/32-bit ARM7TDMI-S microcontroller in a tiny LQFP64 package.
- v 8 KB to 40 KB of on-chip static RAM and 32 KB to 512 KB of on-chip flash memory.
- 128-bit wide interface/accelerator enables high-speed 60 MHz operation.
- In-System Programming/In-Application Programming (ISP/IAP) via on-chip boot loader software. Single flash sector or full chip erase in 400 ms and programming of 256 bytes in 1 ms.
- Embedded ICE RT and Embedded Trace interfaces offer real-time debugging with the on-chip Real Monitor software and high-speed tracing of instruction execution.
- USB 2.0 Full-speed compliant device controller with 2 KB of endpoint RAM.
- In addition, the LPC2146/48 provides 8 KB of on-chip RAM accessible to USB by DMA.
- One or two (LPC2141/42 vs. LPC2144/46/48) 10-bit ADCs provide a total of 6/14analog inputs, with conversion times as low as 2.44 ms per channel.

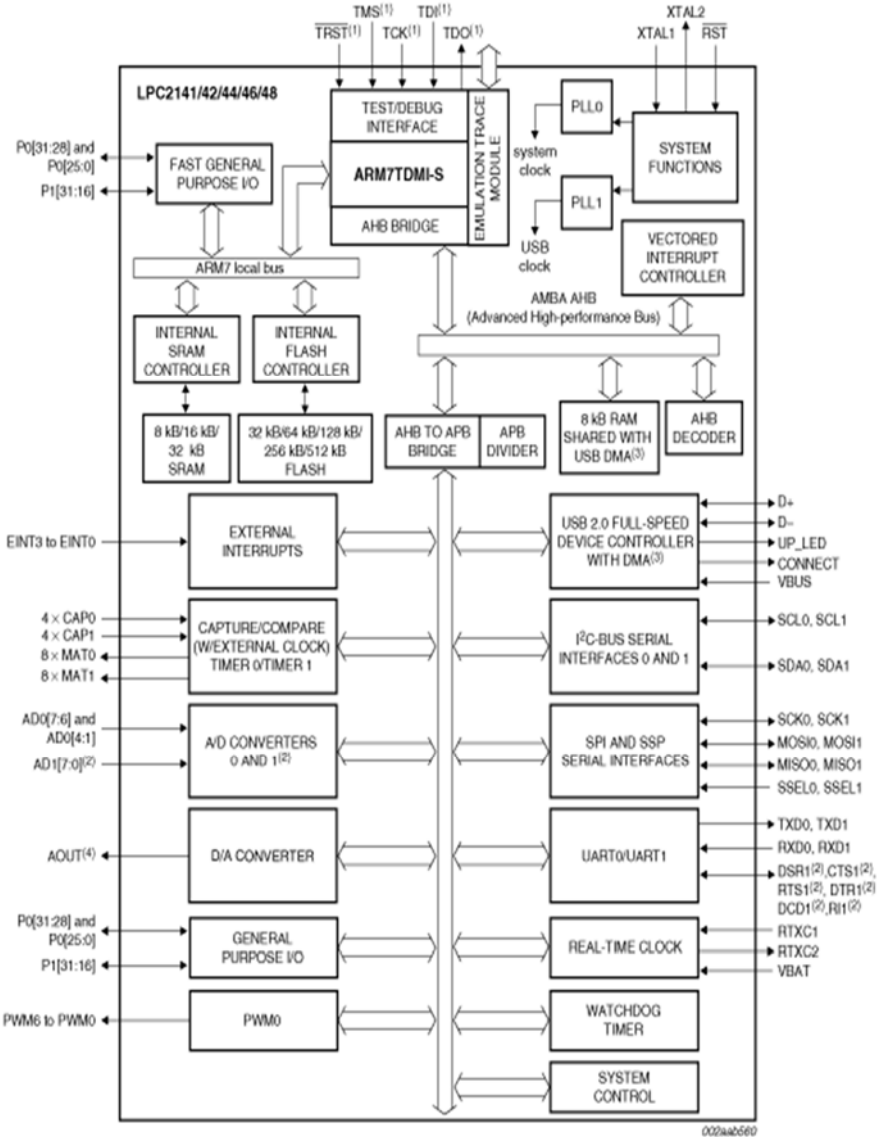

Fig 2: Pin diagram of LPC2148

- Single 10-bit DAC provides variable analog output (LPC2142/44/46/48 only).
- Two 32-bit timers/external event counters (with four capture and four compare channels each), PWM unit (six outputs) and watchdog.
- Low power Real-Time Clock (RTC) with independent power and 32 kHz clock input.
- Multiple serial interfaces including two UARTS (16C550), two Fast I2C-bus (400 Kbit/s), SPI and SSP with buffering and variable data length capabilities.
- Vectored Interrupt Controller (VIC) with configurable priorities and vector addresses.
- Up to 45 of 5 tolerant fast general purpose I/O pins in a tiny LQFP64 package.
- Up to 21 external interrupt pins available.
- 60 MHz maximum CPU clock available from programmable on-chip PLL with settling time of 100 ms.
- On-chip integrated oscillator operates with an external crystal from 1 MHz to 25 MHz.
- Power saving modes include Idle and Power-down.
- Individual enable/disable of peripheral functions as well as peripheral clock scaling for additional power optimization.
- Processor wake-up from Power-down mode via external interrupt or BOD.
- Single power supply chip with POR and BOD circuits: CPU operating voltage range of 3.0 V to 3.6 V (3.3 V ± 10 %) with 5 V tolerant I/O pads.

2.3. XBEE: The XBEE and XBEE-PRO OEM RF Modules were engineered to meet IEEE 802.15.4 standards and support the unique needs of low-cost, low-power wireless sensor networks. The modules require minimal power and provide reliable delivery of data between devices. The modules operate within the ISM 2.4 GHz frequency band and are pin-for-pin compatible with each other.

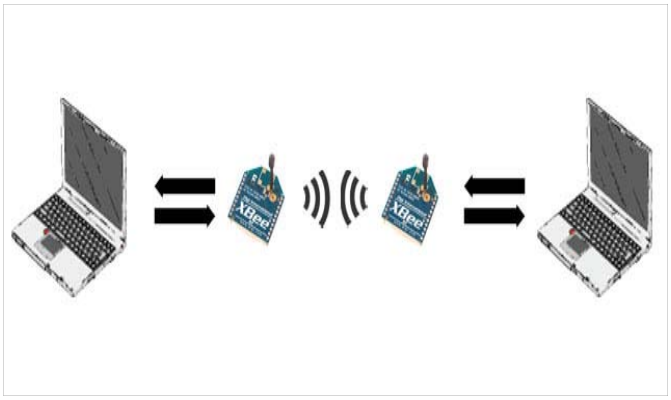

Fig 3: Zigbee module

2.4. Dot Matrix Liquid Crystal Display Controller/Driver The HD44780U dot-matrix liquid crystal display controller and driver LSI displays alpha numeric, Japanese kana characters, and symbols. It can be configured to drive a dot-matrix liquid crystal display under the control of a 4- or 8-bit microprocessor. Since all the functions such as display RAM, character generator, and liquid crystal driver, required for driving a dot-matrix liquid crystal display are internally provided on one chip, a minimal system can be interfaced with this controller/driver. A single HD44780U can display up to one 8-character line or two 8 character lines. The HD44780U has pin function compatibility with the HD44780S which allows the user to easily replace an LCD-II with an HD44780U. The HD44780U character generator ROM is extended to generate 208 5 ´ 8 dot character fonts and 32 5 ´ 10 dot character fonts for a total of 240 different character fonts. The low power supply (2.7V to 5.5V) of the HD44780U is suitable for any portable battery-driven product requiring low power dissipation.

2.5. Power supply unit: This supplies power to the entire circuit. Here we use a step down transformer to obtain the voltage from the mains. This unregulated voltage is regulated using full wave rectifiers and regulators, to obtain required voltage.

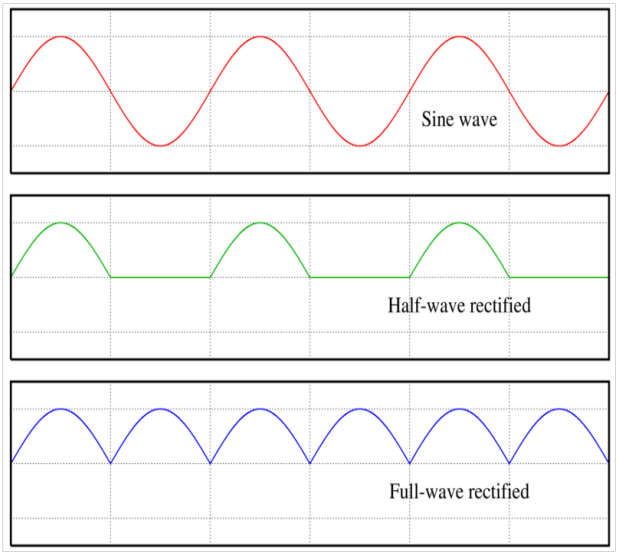

Fig 4: Input and output waveform

2.6. Serial communications: The purpose of this application note is to attempt to describe the main elements in Serial Communication. This application note attempts to cover enough technical details of RS232, RS422 and RS485.

2.6.1. DCE and DTE Devices: DTE stands for Data Terminal Equipment, and DCE stands for Data Communications Equipment. These terms are used to indicate the pin-out for the connectors on a device and the direction of the signals on the pins. Your computer is a DTE device, while most other devices such as modem and other serial devices are usually DCE devices. RS-232 has been around as a standard for decades as an electrical interface between Data Terminal Equipment (DTE) and Data Circuit-Terminating Equipment (DCE) such as modems or DSUs. It appears under different incarnations such as RS-232C, RS-232D, V.24, V.28 or V.10. RS-232 is used for asynchronous data transfer as well as synchronous links such as SDLC, HDLC, Frame Relay and X.25.

2.6.2. Synchronous data transfer: In program-to-program communication, synchronous communication requires that each end of an exchange of communication respond in turn without initiating a new communication. A typical activity that might use a synchronous protocol would be a transmission of files from one point to another. As each transmission is received, a response is returned indicating success or the need to resend.

2.6.3. Asynchronous data transfer: The term asynchronous is usually used to describe communications in which data can be transmitted intermittently rather than in a steady stream. For example, a telephone conversations asynchronous because both parties can talk whenever they like. If the communication were synchronous, each party would be required to wait a specified interval before speaking. The difficulty with asynchronous communications is that the receiver must have a way to distinguish between valid data and noise. In computer communications, this is usually accomplished through a special start bit and stop bit at the beginning and end of each piece of data. For this reason, asynchronous communication is sometimes called start-stop transmission.

2.6.4. RS232: RS-232 (Recommended standard-232) is a standard interface approved by the Electronic Industries Association (EIA) for connecting serial devices. In other words, RS-232 is a long established standard that describes the physical interface and protocol for relatively lowspeed serial data communication between computers and related devices. An industry trade group, the Electronic Industries Association (EIA), defined it original for teletypewriter devices. In 1987, the EIA released a new version of the standard and change the name to EIA-232-D. Many people, however, still refer to the standard as RS 232C, or just RS-232. RS-232 is the interface that your computer uses to talk to and exchange data with your modem and other serial devices. The serial ports on most computers use a subset of the RS- 232C standard.

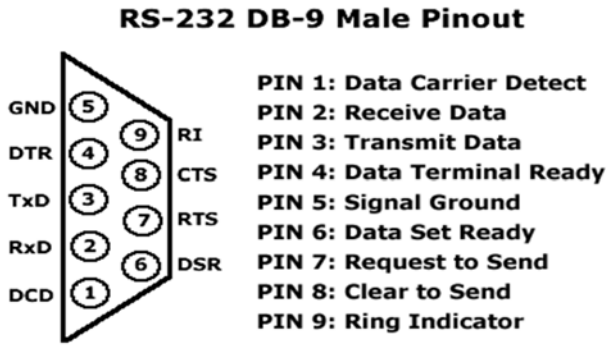

Fig: 5 Pin out of RS-232

3. Functional Discription

3.1. Architectural overview: The ARM7TDMI-S is a general purpose 32-bit microprocessor, which offers high performance and very low power consumption. The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles, and the instruction set and related decode mechanism are much simpler than those of micro programmed Complex Instruction Set Computers (CISC). This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective processor core. The ARM7TDMI-S processor also employs a unique architectural strategy known as Thumb, which makes it ideally suited to high-volume applications with memory restrictions, or applications where code density is an issue.

The key idea behind Thumb is that of a super-reduced instruction set. Essentially, the ARM7TDMI-S processor has two instruction sets: • The standard 32-bit ARM set. • A 16-bit Thumb set.

3.2. On-chip flash program memory: The LPC2141/42/44/46/48 incorporate a 32 KB, 64 KB, 128 KB, 256 KB and 512 KB flash memory system respectively. This memory may be used for both code and data storage. Programming of the flash memory may be accomplished in several ways. It may be programmed In System via the serial port. The application program may also erase and/or program the flash while the application is running, allowing a great degree of flexibility for data storage field firmware upgrades, etc.

3.3. On-chip static RAM: On-chip static RAM may be used for code and/or data storage. The SRAM may be accessed as 8-bit, 16-bit, and 32-bit. The LPC2141, LPC2142/44 and LPC2146/48Page 28 provide 8 KB, 16 KB and 32 KB of static RAM respectively. In case of LPC2146/48 only, an 8 KB SRAM block intended to be utilized mainly by the USB can also be used as a general purpose RAM.

3.4. Interrupt controller: The Vectored Interrupt Controller (VIC) accepts all of the interrupt request inputs and categorizes them as Fast Interrupt Request (FIQ), vectored Interrupt Request (IRQ), and non-vectored IRQ as defined by programmable settings. The programmable assignment scheme means that priorities of interrupts from the various peripherals can be dynamically assigned and adjusted.

3.5. Fast general purpose parallel I/O: Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back, as well as the current state of the port pins.

3.6. 10-bits ADC:

- 10 bit successive approximation analog to digital converter.
- Measurement range of 0 V to 2.0 V.
- Each converter capable of performing more than 400,000 10-bit samples per second.
- Every analog input has a dedicated result register to reduce interrupt overhead.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition on input pin or timer match signal.
- Global Start command for both converters (LPC2142/44/46/48 only).

3.7. 10-bit DAC: The DAC enables the LPC2141/42/44/46/48 to generate a variable analog output. The maximum DAC output voltage is the VREF voltage.

- 10-bit DAC.
- Buffered output.
- Power-down mode available.

3.8. USB 2.0 device controller: The USB is a 4-wire serial bus that supports communication between a host and a number (127 max) of peripherals.

- Fully compliant with USB 2.0 Full-speed specification.
- Supports 32 physical (16 logical) endpoints.
- Supports control, bulk, interrupt and isochronous endpoints.

- Scalable realization of endpoints at run time.
- RAM message buffer size based on endpoint realization and maximum packet size.
- Supports Soft Connect and Good Link LED indicator. These two functions are sharing one pin.
- Supports bus-powered capability with low suspend current.
- Supports DMA transfer on all non-control endpoints (LPC2146/48 only).
- One duplex DMA channel serves all endpoints (LPC2146/48 only).
- Allows dynamic switching between CPU controlled and DMA modes (only in LPC2146/48).
- Double buffer implementation for bulk and isochronous endpoints.

3.9. UARTS: The LPC2141/42/44/46/48 each contain two UARTS. In addition to standard transmit and receive data lines, the LPC2144/46/48 UART1 also provides a full modem control handshake interface.

- 16 byte Receive and Transmit FIFOS.
- Register locations conform to '550 industry standard.
- Receiver FIFO trigger points at 1, 4, 8, and 14 bytes.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Transmission FIFO control enables implementation of software (XON/XOFF) flow control on both UARTS.

3.10. I2C-bus serial I/O controller: The LPC2141/42/44/46/48 each contain two I2C-bus controllers.

- Compliant with standard I2C-bus interface.
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I2C-bus can be used for test and diagnostic purposes.

4. Modes of Operation: XBEE/XBEE-PRO RF Modules operate in five modes.

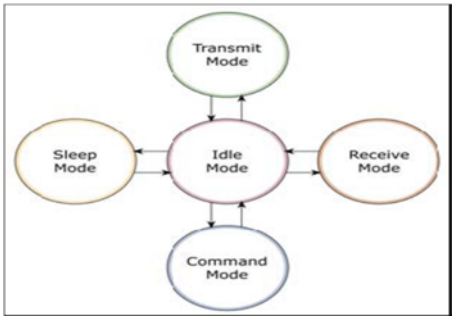

Fig 6: Modes of operation

1. Idle Mode: When not receiving or transmitting data, the RF module is in Idle Mode.
2. Transmit Mode:Serial data is received in the DI Buffer.
3. Receive Mode :Valid RF data is received through the antenna.
4. Sleep Mode :Sleep Mode condition is met.
5. Command Mode:Command Mode Sequence is issued.

5. Scope of Study

- Vehicles identification at VIPs places.
- Eg PARLIAMENT, VIPs HOMES, HOTELS (all high level hotels) and apartments.

6. Conclusion

The proposed XBee technology based on Wireless Vehicle identification and driver authentication system satisfies the much needed requirement of vehicle security.Use of XBee module ensures the system to be low cost and low power consumable system. · User-friendly interface and simple system setup. Xbee Wirless Vehicular Identification And Authentication security based systems is a big break though in the security field. Ø Minimize militant attacks like whatever had happened in the parliament, hotel Taj and hotel Oberio.

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