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## Lower order harmonics removal in a grid-connected PV inverter

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### Abstract

Now-a-days the development of distributed generation systems is in progress. With exhaustion of the conventional resources such as coal, oil etc, there is a constant demand for the distributed generation systems which mainly use renewable energy resources. When a DG source is being connected to the grid, there are many constraints to be met one of which is the harmonic content of the current being injected into the grid. This paper deals mainly with building a Multisim Simulation model to mitigate lower order harmonics using adaptive harmonic elimination technique. In this paper, filters are designed to eliminate only the higher order harmonics and to mitigate lower order harmonics, an adaptive selective harmonic elimination technique (AHE) is used. The total control of the system is done using Lab View & NI DAQ and the output is compared and integrated with Multisim Simulated results.

**Keywords:** solar energy, buck-boost converter, inverter, LMS Adaptive filters, harmonic distortion

### 1. Introduction

Use of Renewable energy sources (solar, wind, geothermal etc) is becoming very important in electric power generation due to the depletion of conventional energy sources (coal gas etc.). Many distributed generation systems making use of this renewable energy are being designed and are connected to grid. The objective of this paper is to design a power converter suitable for a DGS using solar panels as the energy source and control its operation using NI DAQ. Fig.1 shows the designing of power circuit. The design of the power circuit is done by using Multisim. The design process of the circuit is done when the control signal is processed from Lab View. Multisim is a spice based simulation tool and it can be used for simulation and even can be used to get the real time data via NI DAQ. Lab View is a Measurement and Control software which is used for real time measurement and control application. Generally all type of the real time industrial application requires measurement and control. So Lab View can be used for versatile environment. The complete system data are measured and the Harmonic control is done by using Lab View & NI DAQ. The Harmonic reduction is done by using **Adaptive** filter. As the design of power circuit is done using solar panels as the source, a buck-boost stage is required to convert variable DC voltage to fixed dc voltage by using Lab View so that we get fixed DC voltage at the output of Buck-Boost Converter and control of the system is done using Lab-View. The buck-boost stage is followed by the single phase H-bridge inverter. The inverter switches are MOSFETs. Output of the inverter is connected to the filter (either L or LC) to remove harmonics present in it. Harmonics are of two types namely higher order and lower order harmonics. Thus to remove these Harmonics filters are designed. However, in real systems, lower order harmonics are also present in the system. Ideally the system showed in Fig1 will not have lower order harmonics. The following factors are responsible for generation of lower order harmonics in system [1]:

1. The gap-time or blanking time introduced between the switching of devices of the same leg to avoid short circuiting [2].
2. The on-state voltage drops on the switching devices.
3. The magnetizing current, which is usually very rich in lower order harmonics by the transformer, is responsible for generation of lower order harmonics.

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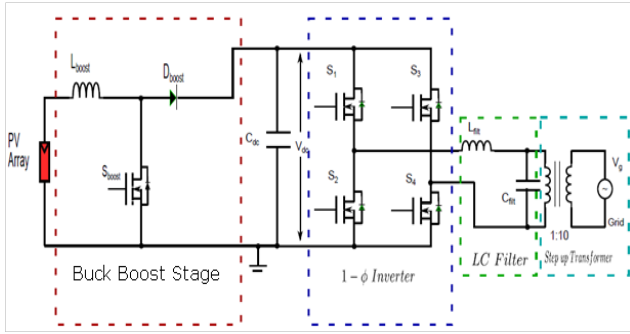


Fig 1: Design Interface of Power Circuit [2]

In order to remove these lower order harmonic in the system, a simple method or solution is to increase the size of the filter. But this increase in size of filters will make filter bulky by increasing its overall costing. Thus in this paper, an adaptive harmonic elimination technique (AHE) based LMS Algorithm [2] is used to limit the injection of these harmonics into the system. The adaptive harmonic technique estimates and attenuates a particular harmonic in the output current.

The organization of this paper is as follows: Section II discusses the origin of lower order harmonics generation in system. In Section III, the concept of adaptive harmonic compensation is explained. Section IV discusses design methodology in detail. It describes the general block diagram of system and also its implementation. In Section V, results are provided. Conclusions are given in Section VI.

**2. Sources of Lower Order Harmonics**

Unlike the other practical devices in an inverter circuit the switching of the devices is complementary, especially of the devices on the same leg. Hence we can say that if the same complementary pulses are given to the devices at the same time, then it will lead to a period of time when any two devices of the same leg will be ON simultaneously which would in turn result in the undesirable shorting of the DC bus. Therefore, it is important to introduce a gap time between the switching of the devices. Gap time or dead time is hence the time during which a device which is ON will be switched OFF. It means that a turned OFF device will be turned ON only after dead time. The dead or gap time  $t_d$  has to be at least equal to the turn-OFF time in devices. The error voltages due to the dead time / gap time for switches S3 – S4 will be the same as that of switches S1 – S2 but there would be a phase lag of 180°. Thus, it is evident from the features of the waveform that, since the applied voltage is a square wave, lower order harmonics will be infused into the grid. This error voltage is responsible for injecting of lower order harmonics currents into the grid. Each odd harmonic that is installed will be 180° out of phase with respect to the inductor current. The employment of a bulky filter will decrease this, but in this project an adaptive technique is used to reduce it.

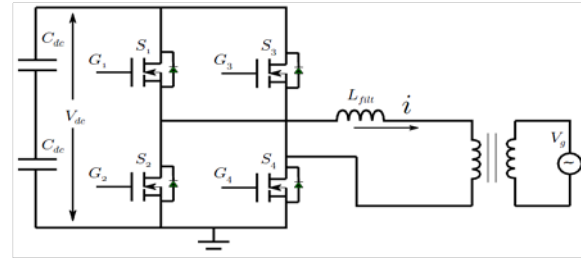


Fig 2: Schematic 1-phase inverter

**3. Adaptive Harmonic Compensation**

Certain filters have a very distinct quality of modifying their parameters or coefficients according to some algorithms, such filters are known as Adaptive filters. Their settlement or compensation for the sinusoidal interference signal is a critical application worth mentioning. One of the enticing features of the adaptive filters is that it can adapt to time varying system characteristics. In this paper, adaptive filters whose coefficients are changed as per Least Mean Square (LMS) algorithm are used. Fig 3 illustrates a general adaptive filter with N coefficients (weights). The weights are adapted by using LMS algorithm

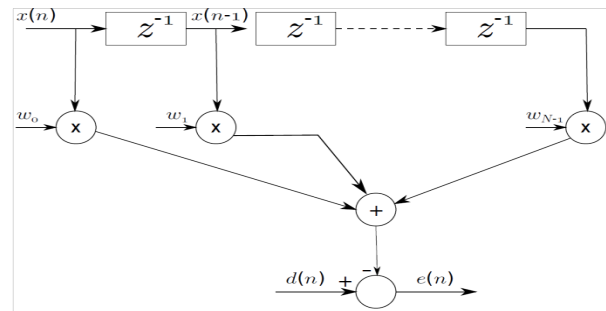


Fig 3: General adaptive filter [2]

For Fig 3 coefficient vector is defined as:

$$\vec{w} = [w_0 \ w_1 \ \dots \ w_{N-1}]^T \dots \dots \dots (1)$$

Input vector and filter output are given in Equations 2 and 3

$$\vec{x}(n) = [x(n) \ x(n-1) \ \dots \ x(n-N+1)]^T \dots \dots \dots (2)$$

$$y(n) = \vec{w}^T \vec{x}(n) \dots \dots \dots (3)$$

The error signal is,

$$e(n) = d(n) - y(n) \dots \dots \dots (4)$$

A performance function is defined as

$$\zeta = E[s^2(n)] \dots \dots \dots (5)$$

In any adaptive filter, the weight vector  $\vec{w}$  is updated such that the performance function moves towards its global minimum. Thus the updating of weights would be done as,

$$\vec{w}(k+1) = \vec{w}(k) - \mu \nabla_k \zeta \dots \dots \dots (6)$$

In Equation 6  $\mu$  = step size. The convergence of the adaptive filter depends on the step size. A smaller value would make the adaption process very slow whereas a large value would make the system oscillatory. When the global minimum of  $\zeta$  is reached,  $\nabla\zeta$  would be zero and there would not be anymore adaption in weights. The generalized algorithm mentioned above applies to all adaptive filters. LMS adaptive filters incorporate a slight modification in algorithm as in the performance function which is the expectation of error squared is approximated to be the error squared itself. Thus, for an LMS adaptive filter, the performance function would be,

$$\zeta = e^2(n) \dots \dots \dots (7)$$

From Equation 7, the update equation for LMS algorithm can be deduced. Eqn. 6 would change as

$$\bar{w}(n+1) = \bar{w}(n) + \mu \nabla e^2(n) \dots \dots \dots (8)$$

$\nabla$  is defined as the gradient with respect to the weights of the filter. Thus,

$$\nabla = \left[ \frac{\partial}{\partial w_0} \quad \frac{\partial}{\partial w_1} \quad \dots \quad \frac{\partial}{\partial w_{N-1}} \right] \dots \dots \dots (9)$$

It can be written that,

$$\frac{\partial e^2(n)}{\partial w_i} = 2e(n) \frac{\partial e(n)}{\partial w_i} \dots \dots \dots (10)$$

From Equation 4 and by the assumption that input  $d(n)$  is independent of weights, Equation 10 would change as

$$\frac{\partial e^2(n)}{\partial w_i} = -2e(n)x(n-i) \dots \dots \dots (11)$$

Or,

$$\nabla e^2(n) = -2e(n)\bar{x}(n) \dots \dots \dots (12)$$

Combining Equation 2 and Equation 8, the final update equation for weights of an LMS adaptive filter is obtained, which is

$$\bar{w}(n+1) = \bar{w}(n) + 2\mu e(n)\bar{x}(n) \dots \dots \dots (13)$$

Thus, the following steps are used to estimate the maximum step size value for an adaptive filter.

1. Obtains a series of filter input vectors from the input signal.
2. Identifies the filter input vector that has the maximum signal power.
3. Calculates the reciprocal of the maximum signal power. The result is the maximum step size that can be used for the adaptive filter.

#### 4. Design Methodology

PV system consists of DC-DC Buck- Boost Converter, Single Phase Inverter, Filter and Single Phase Transformer as shown in Fig 4.

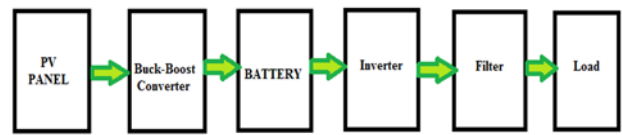


Fig 4: General Block diagram of the PV System

PV Module produces the Variable DC Power output; this Variable DC is converted into Fixed DC voltage by using Buck-Boost Converter and the control is done using Lab View so that we get fixed DC voltage at the output of Buck-Boost Converter. Then DC power is transferred to Inverter. This inverter further converts DC power to AC power. Output of the inverter is connected to the filter (either L or LC) to remove harmonics present in it. Ideally, PWM of switches shifts all the harmonics to switching frequency and its multiples. Thus Filters are designed to eliminate only the higher order harmonics and to mitigate lower order harmonics, an adaptive selective harmonic elimination technique (AHE) is used. The total control of the system is done using Lab View & NI DAQ. The final resultant output is a harmonic eliminated output.

##### A. DC-DC CONVERTER:

PV system consists of the DC-DC converter, this converter is directly connected to the PV module. In DC-DC Converter Topology, different types of converter topologies are available, but in this paper a Buck - Boost Topology is used. This Converter is used to convert the Variable DC output taken from the PV module into fixed DC output. A buck-boost converter provides an output voltage that may be less than or greater than the input voltage hence the name “buck-boost”. The circuit arrangement of a buck-boost converter is shown in Fig 5. This Buck-Boost converter is made of switching devices (MOSFET) [8].

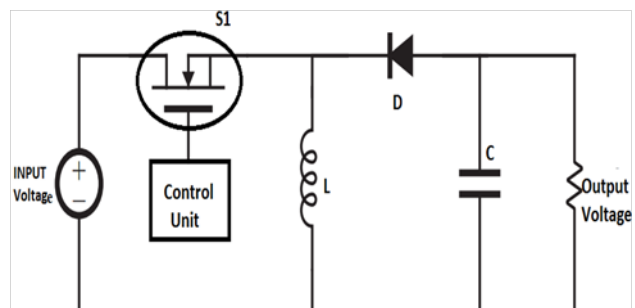


Fig 5: Buck-Boost Converter diagram

Buck-Boost Converter topology consists of a switching device S1 which is been controlled by control unit circuit so that we get desired fixed DC output voltage, a diode D, an inductor L, and a filter capacitor C. As shown in Fig 5 the operation of the circuit is been divided into two operating modes. During first operating mode, switching device S1 is turned on for a given input voltage and diode D is in blocking mode i.e. reverse biased. Hence flow of current is from input voltage<sup>+</sup> – switch S1 – inductor L - input voltage<sup>-</sup>. Due to presence inductor L, inductor L stores energy during these mode and input current rises. In mode 2, switching device S1 is turned off and the current which was flowing

through inductor L, will now flow through inductor L, capacitor C, and diode D, and the load. Hence stored energy in inductor L is transferred to the load connected at output. Next cycle begins as raised inductor current becomes zero and therefore switching device S1 is turns on again and cycle repeats. During on time  $T_{on}$ , input energy to inductor from the source is given by,

$$W_i = V_{in} \cdot I_s \dots \dots \dots (1)$$

During off time  $T_{off}$ , released energy from the inductor is given by,

$$W_o = V_o \cdot I_s \cdot T_{off} \dots \dots \dots (2)$$

For a lossless system in steady state condition,

Input energy,  $W_i$  = Output energy  $W_o$

Therefore equating equation 1 & equation 2 we get,

$$V_o = V_{in} \cdot \alpha / 1 - \alpha$$

When  $\alpha < 0.5$ , say  $\alpha = 0.3$  then,  $V_o < V_{in}$ .

When  $\alpha > 0.5$ , say  $\alpha = 0.7$  then,  $V_o > V_{in}$ .

Thus depending on the value of duty cycle the output voltage can be more or less than the given input voltage. As PV Module produces the Variable DC Power output; this Variable DC is converted into Fixed DC voltage by using Lab View so that we get fixed DC voltage at the output of Buck-Boost Converter. Table below shows the value of duty cycle adjusted in Lab View so that we get fixed DC output voltage.

Input Voltage	Desired Fixed Output Voltage	Duty Cycle
9V	15 V	62%
10V	15 V	60%
11V	15 V	57%
12V	15 V	55%
13V	15 V	53%
14V	15 V	51%
15V	15 V	50%
16V	15 V	48%
17V	15 V	46%
18V	15 V	45%
19V	15 V	44%
20V	15 V	42%
21V	15 V	41%
22V	15 V	40%
23V	15 V	39%
24V	15 V	38%
25V	15 V	37%

Table no 1: Duty Cycle Chart

To calculate the power stage of a converter, following parameters are considered:

Input voltage range:  $V_{inmin} = 9V$ .

$V_{inmax} = 25V$ .

Nominal output voltage:  $V_{out} = 15V$ .

**I) Calculation of Duty Cycle:**

$$D_{buck} = \frac{V_{out} \times \eta}{V_{inmax}}$$

$$= 15 \times 0.8 / 30$$

$$= 0.4$$

$$D_{boost} = 1 - \frac{V_{inmin} \times \eta}{V_{out}}$$

$$= 1 - ((9 \times 0.8) / 15)$$

$$= 1 - 0.48$$

$$= 0.52$$

**II) Calculating Inductor Value “L”**

**LBUCK**

$$L > \frac{V_{out} \times (V_{inmax} - V_{out})}{K_{ind} \times F_{sw} \times V_{inmax} \times I_{out}}$$

Where:

$V_{inmax}$  = maximum input voltage.

$V_{out}$  = desired output voltage.

$I_{out}$  = desired maximum output current.

$F_{sw}$  = switching frequency of the converter.

$K_{ind}$  = estimated coefficient that represents the amount of inductor ripple current relative to the maximum output current. A good estimation for the inductor ripple current is 20% to 40% of the output current, or  $0.2 < K_{ind} < 0.4$ .

$K_{ind} = 0.3$ .

$$L = ((15 \times (30 - 15)) / (0.3 \times 1000 \times 30 \times 2))$$

$$L = 0.01mh$$

**LBOOST**

$$L > \frac{V_{inmin}^2 \times (V_{out} - V_{inmin})}{F_{sw} \times K_{ind} \times I_{out} \times V_{out}^2}$$

Where:

$V_{inmin}$  = minimum input voltage.

$V_{out}$  = desired output voltage.

$I_{out}$  = desired maximum output current.

$F_{sw}$  = switching frequency of the converter.

Kind = estimated coefficient that represents the amount of inductor ripple current relative to the maximum output current. A good estimation for the inductor ripple current is 20% to 40% of the output current, or  $0.2 < Kind < 0.4$ .

$$L = \frac{((9^2) \times (15-9))}{((15^2) \times 2 \times 0.3 \times 1000)}$$

$$L = 0.0036\text{mh}$$

III) Max. Switching current

**Buck Mode:**

$$I_{swmax} = \frac{\Delta I_{max}}{2} + I_{out}$$

$$\Delta I_{max} = \frac{(V_{inmax} - V_{out}) \times D_{buck}}{F_{sw} \times L}$$

$$I_{sw} = 2.24\text{A}$$

**Boost Mode:**

$$I_{swmax} = \frac{\Delta I_{max}}{2} + \frac{I_{out}}{1 - D_{boost}}$$

$$\Delta I_{max} = \frac{V_{inmin} \times D_{boost}}{F_{sw} \times L}$$

$$I_{sw} = 4.8\text{A}$$

IV) Calculating Capacitor Value “C”

**Buck mode:**

$$C_{outmin1} = \frac{K_{ind} \times I_{out}}{8 \times F_{sw} \times V_{out\_ripple}}$$

$$= \frac{(0.3 \times 2)}{(8 \times 14000 \times 1)}$$

$$= 0.000075\text{mf}$$

$$C_{outmin2} = \frac{(K_{ind} \times I_{out})^2 \times L}{2 \times V_{out} \times \Delta V_{out}}$$

$$= 0.00024\text{mf}$$

**Boost mode:**

$$C_{outmin} = \frac{I_{out} \times D_{boost}}{F_{sw} \times \Delta V_{out}}$$

$$\Delta V_{out\_esr} = ESR \times \left( \frac{I_{out}}{1 - D_{boost}} + \frac{K_{ind} \times I_{out} \times V_{out}}{2 \times V_{in}} \right)$$

$$= 0.00024\text{mf}$$

The Model shown in Fig 6 is simulated using Multisim and Lab View. The plots obtained for buck and boost mode in the different scopes have been shown in Fig 7 and 8. The simulation is taken to be time varying, to reflect real life conditions. The Hardware set-up for the same is shown in Fig 10.

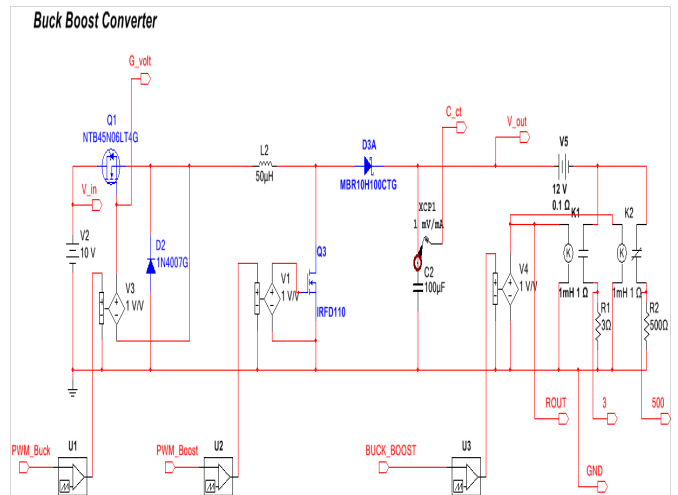


Fig 6: Design of Buck-Boost Converter

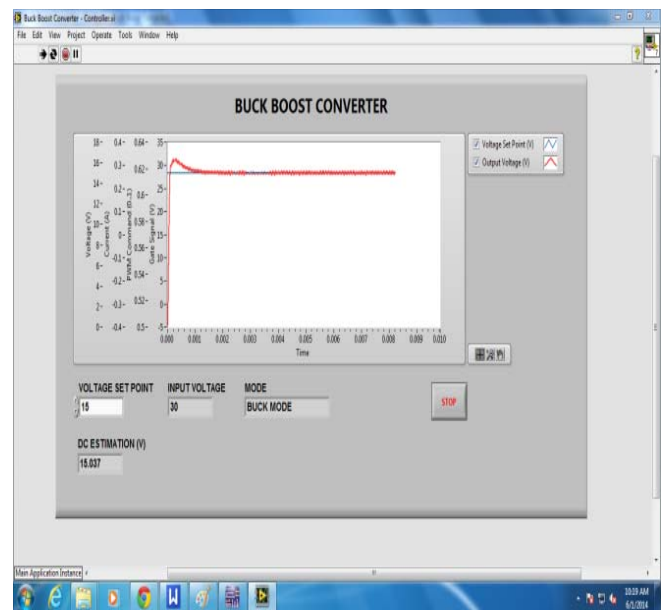


Fig 7: Output Scope during Buck-Mode

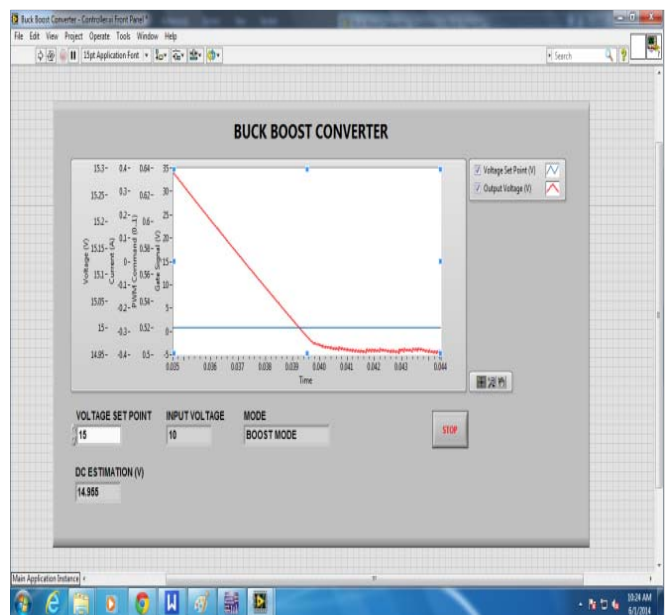


Fig 8: Output Scope during Boost-Mode

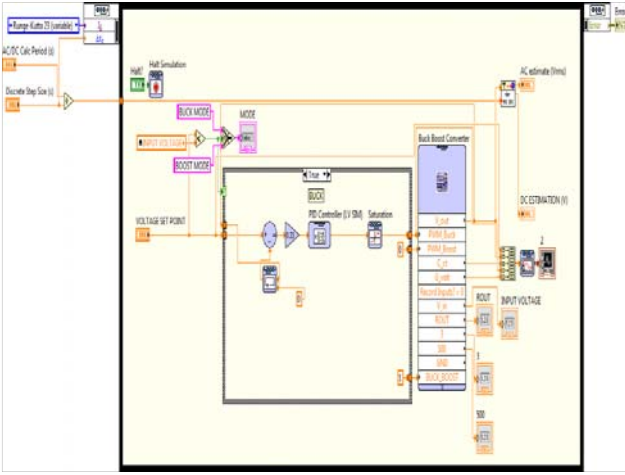


Fig 9: Lab View Program for Buck-Boost

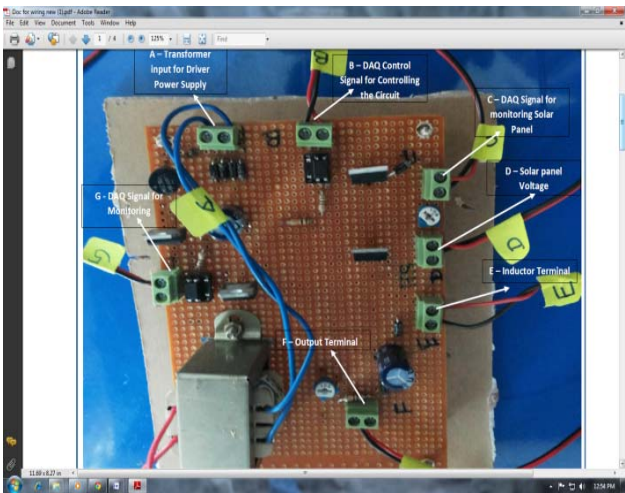


Fig 10: Hardware Implementation of Buck-Boost Converter

- A- Transformer input for Driver Power Supply. (Driver Circuit power supply are connected with transformer)
- B- DAQ Control Signal for Controlling the Circuit.(Buck-Boost Converter control Signal given by using NI DAQ)
- C- DAQ Signal for monitoring Solar Panel. (Solar panel voltage monitoring terminal)
- D- Solar panel Voltage. (Buck- boost converter input terminal main power circuit)
- E- Inductor Terminal.
- F- Output Terminal.

**B. Inverter :**

The conversion of the DC supply to AC is done by the inverter. The conversion of the 12V or 24V DC supply to 240V AC supply is done by our household inverter at a desirable frequency of 50-60 Hz. It can be used in other applications like UPS (uninterruptible power supply), AC motor drives. Now-a-days inverters are used for applications like grid connection of wind energy system or photovoltaic system that is in applications pertaining to renewable energy resources. It consists of two arms with two semiconductor switches on both arms with antiparallel freewheeling diodes for discharging the reverse current. Antiparallel freewheeling diodes are the ones which facilitate the flow of reverse load current. They make a different way for the inductive current to flow during the turn OFF condition. Out of the four

switches in our circuit Q3, Q4, and Q5, Q6, are operated alternately, so that they are not ON/OFF at the same time. This in turn keeps the two switches OFF for a short period of time called as the blanking time and remaining two switches ON, so that short circuiting is prevented. The switching of the bridge legs takes place so that there is change of polarity in the voltage by the shifting of voltage from one to another. If the shift Angle is zero; the output voltage is also zero and maximal when shift angle is  $\pi$ .

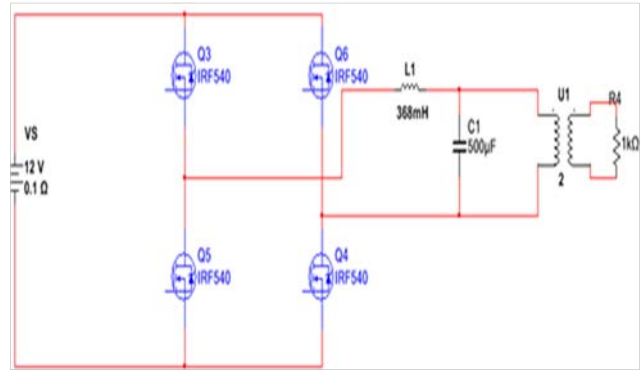


Fig 11: Single Phase Full wave Bridge Inverter

The Model shown in Fig 12 and Fig 13 is simulated using Multisim and Lab View. The inverter output showing 220V AC is shown in Fig 14. The Hardware set-up for the same is shown in Fig 15 and Fig 16.

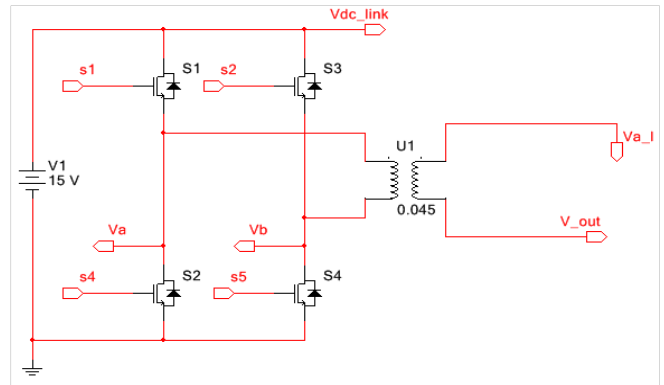


Fig 12: Design of Single Phase H-Bridge Inverter

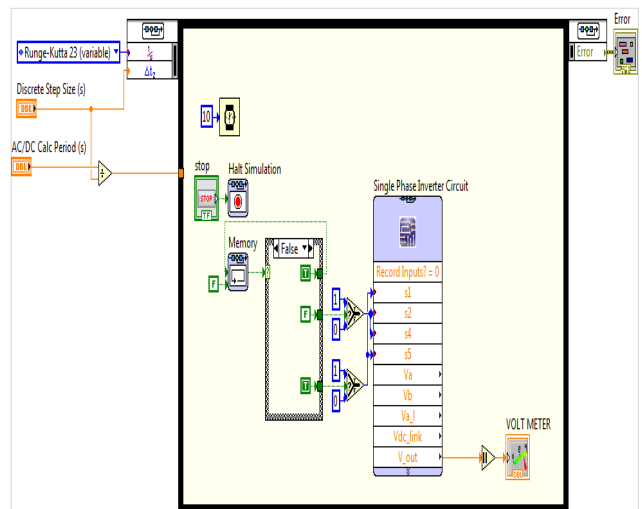


Fig 13: Lab View Program for Single Phase H-Bridge Inverter

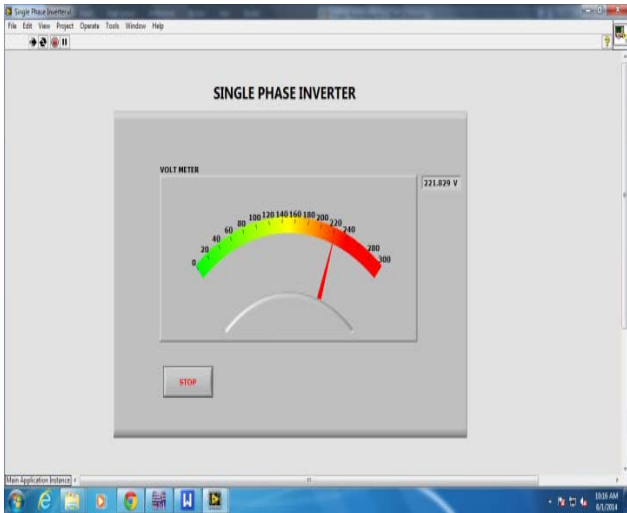


Fig14: Output Scope Showing 220V AC

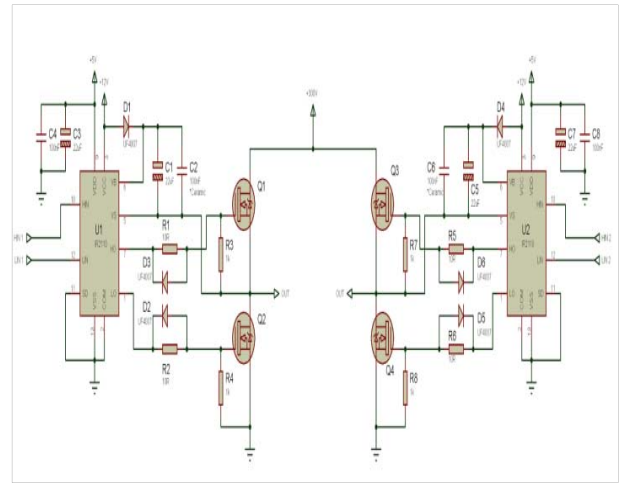


Fig 15: Design of Single Phase Inverter

Table No. 2: Lead Definitions

Lead Definitions	
Symbol	Description
VDD	Logic supply
HIN	Logic input for high side gate driver output (HO), in phase
SD	Logic input for shutdown
LIN	Logic input for low side gate driver output (LO), in phase
VSS	Logic ground
VB	High side floating supply
HO	High side gate drive output
Vs	High side floating supply return
VCC	Low side supply
LO	Low side gate drive output
COM	Low side return

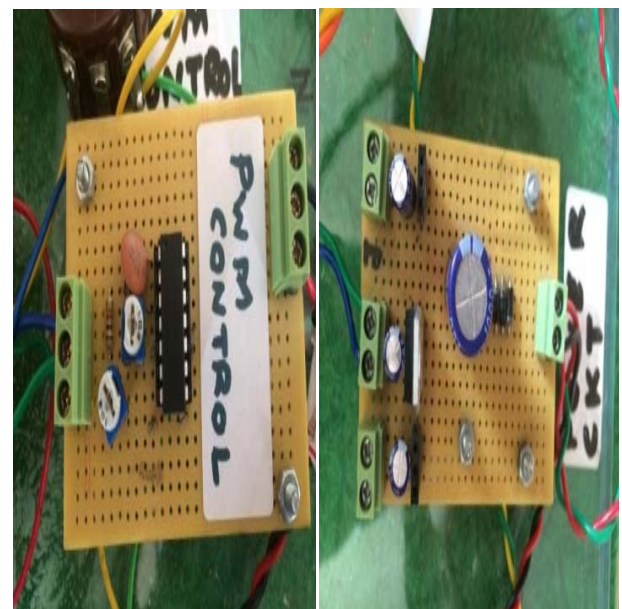
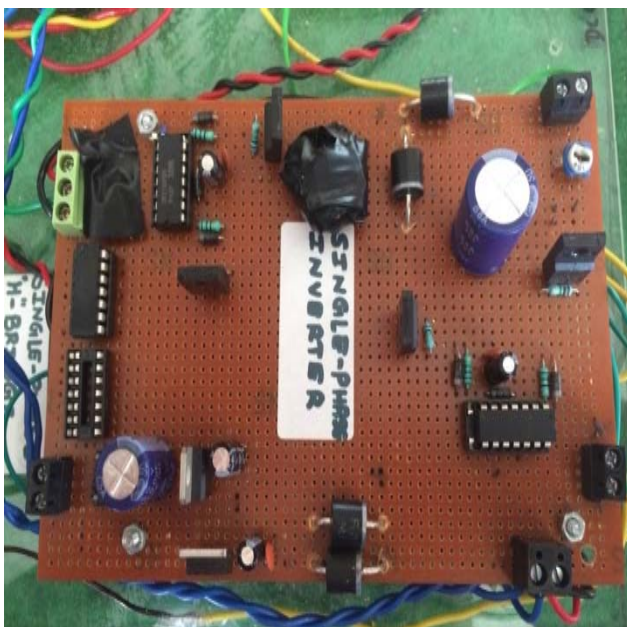


Fig16: Hardware Implementation Single Phase Inverter

**C. LC – Filter:**

A filter (L or LC) is connected at the output of the inverter, as it contains harmonics. The filter, filters-out the higher order harmonics, but in practical systems lower order harmonics are also present. The following factors are responsible for the presence of lower order harmonics: The dead-time introduced between the switching's of devices of the same leg [4] the on-state voltage drops on the switches; the magnetizing current drawn by the transformer is usually rich in lower order harmonics. One solution to this problem is the increase in the filter size but, this makes it bulky. Thus in this project, an adaptive harmonic elimination technique (AHE) [5] is used to limit the injection of these harmonics into the grid. The adaptive harmonic compensation technique is based on the usage of an LMS adaptive filter to estimate a particular harmonic in the output current. This is then used to generate a counter voltage reference using a proportional controller to attenuate that particular harmonic.

The designing of the LC filter involves adjusting the cut-off frequency such that most of the lower order harmonics are eliminated; hence it is connected at the output terminal of Full Bridge VSI to mitigate the harmonics generated by the pulsating modulation waveform. To operate as an ideal voltage Source, that means no additional voltage distortion even though under the load variation or a nonlinear load, the output impedance of the inverter must be kept zero. Therefore, the capacitance value should be maximized and the inductance value should be minimized at the selected cut-off frequency of the low-pass filter. The values of L and C are then found out as these values determine the reactive power which decides the cost of the filter, then it is common that the filter components are determined at the set of a small capacitance and a large inductance and consequently the output impedance of the inverter is so high. These makes the output impedance of the load zero, hence the voltage waveform of the inverter output will be sinusoidal under the linear load or steady state condition. But in case of a step change of the load or a nonlinear load, the output voltage waveform will be distorted because by the slow system response as the output response is non-zero. The kind of the load, such as linear or non-linear will decide the flow of the load current, hence making it is difficult to represent the transfer function of inverter output voltage to load current.

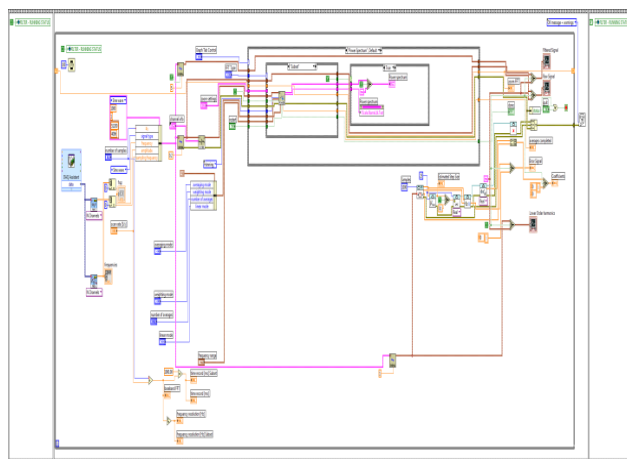


Fig 18: Lab View Program for LMS Adaptive Filter

**5. Results**

Here, simulation results showing use of LC-Filter and LMS Adaptive Filter for removal of lower order harmonics are presented.

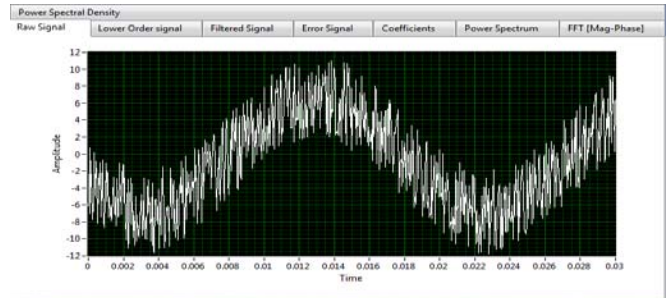


Fig 18: Output Scope Showing Raw Signal

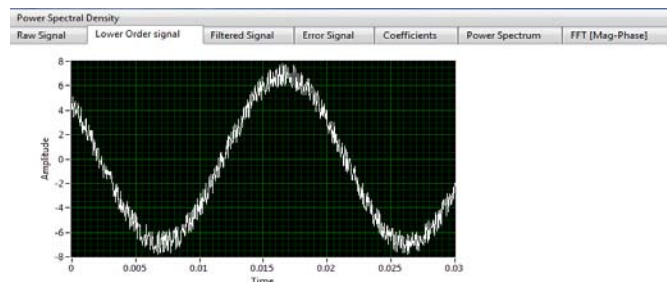


Fig 19: Output Scope Showing Signal with Lower Order Harmonics

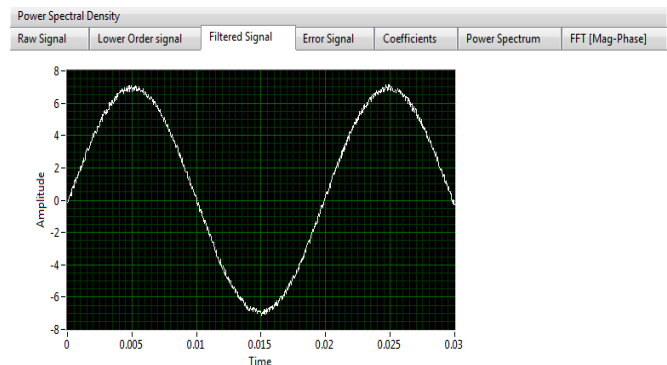


Fig 20: Output Scope Showing Filtered Signal



Fig 21: Output Scope Showing Total Error Signal

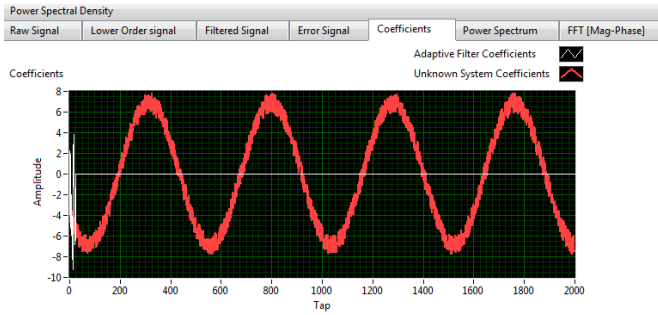


Fig 22: Output Scope Showing Coefficients

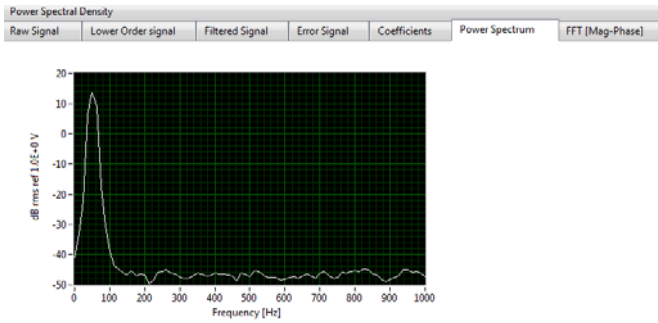


Fig 23: Output Scope Showing Power Spectrum of Signal

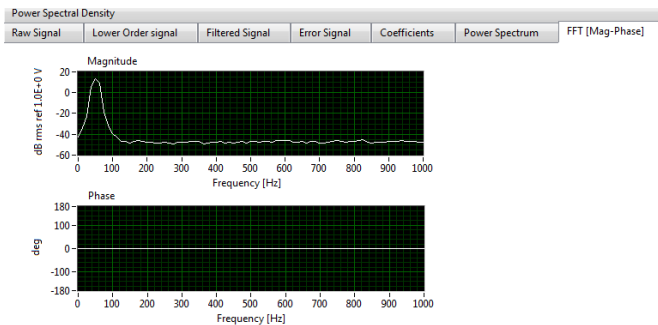


Fig 24: Output Scope Showing FFT of Signal

**6. Conclusions**

One of the crucial issues relating to quality of power and disturbances in power systems is the Harmonic Distortion. This project deals with the elimination of the lower order harmonics by developing hardware set-up and Multisim simulation model. The data acquisition for the entire system and the controlling of the harmonics is done using Lab VIEW and NI-DAQ. The harmonic reduction is done by using Adaptive filter. The Adaptive harmonic elimination technique is based on the usage of a Least Mean Square (LMS) adaptive filter to estimate a particular harmonic in the output current and generate a counter voltage reference to attenuate that particular harmonic. Thus the entire system is controlled and monitored using Lab-View and NI DAQ.

**7. References**

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