International Journal of Multidisciplinary Research and Development
Online ISSN: 2349-4182 Print ISSN: 2349-5979
www.allsubjectjournal.com
Volume 2; Issue 11; November 2015; Page No. 178-180

Tunnel field effect transistor with junctionless structural characteristics & design

Konda Venkata Ashok

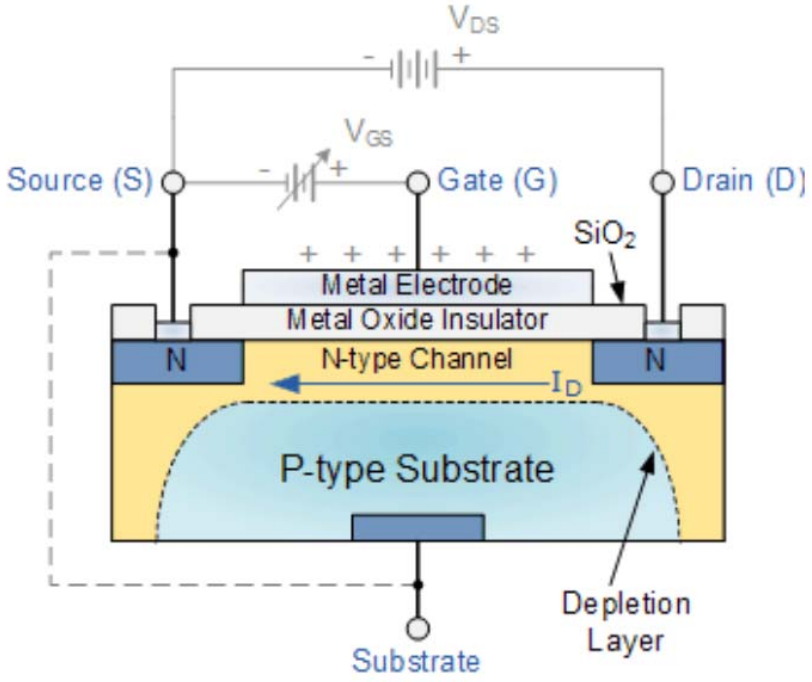
M-Tech, Vlsi Design, Srm University

Abstract
In research paper involves a study of a double-gate junction less tunnel field effect transistor (JL-TFET). The JL-TFET is a Si-channel heavily n-type-doped junction less field effect transistor (JLFET), which uses two isolated gates (Control- Gate, P-Gate) with two different metal work-functions to behave like a tunnel field effect transistor (TFET). The tunnel field-effect transistor (TFET) is a new type of transistor. Even though its structure is very similar to a metal-oxide-semiconductor field-effect (MOSFET), the fundamental switching mechanism differs, making this device a promising candidate for low energy electronics. TFETs switch by modulating quantum tunneling through a barrier instead of modulating thermionic emission over a barrier as in traditional MOSFETs. In this structure, the advantages of JLFET and TFET are combined together. The simulation results of JL-TFET with high-k dielectric material (TiO2) of 20-nm gate length shows excellent characteristics with high ION/IOFF ratio (~6 × 108), a point subthreshold slope (SS) of ~38 mV/decade, and an average SS of ~70 mV/decade at Room temperature, which indicates that JL-TFET is a promising candidate for a switching performance.

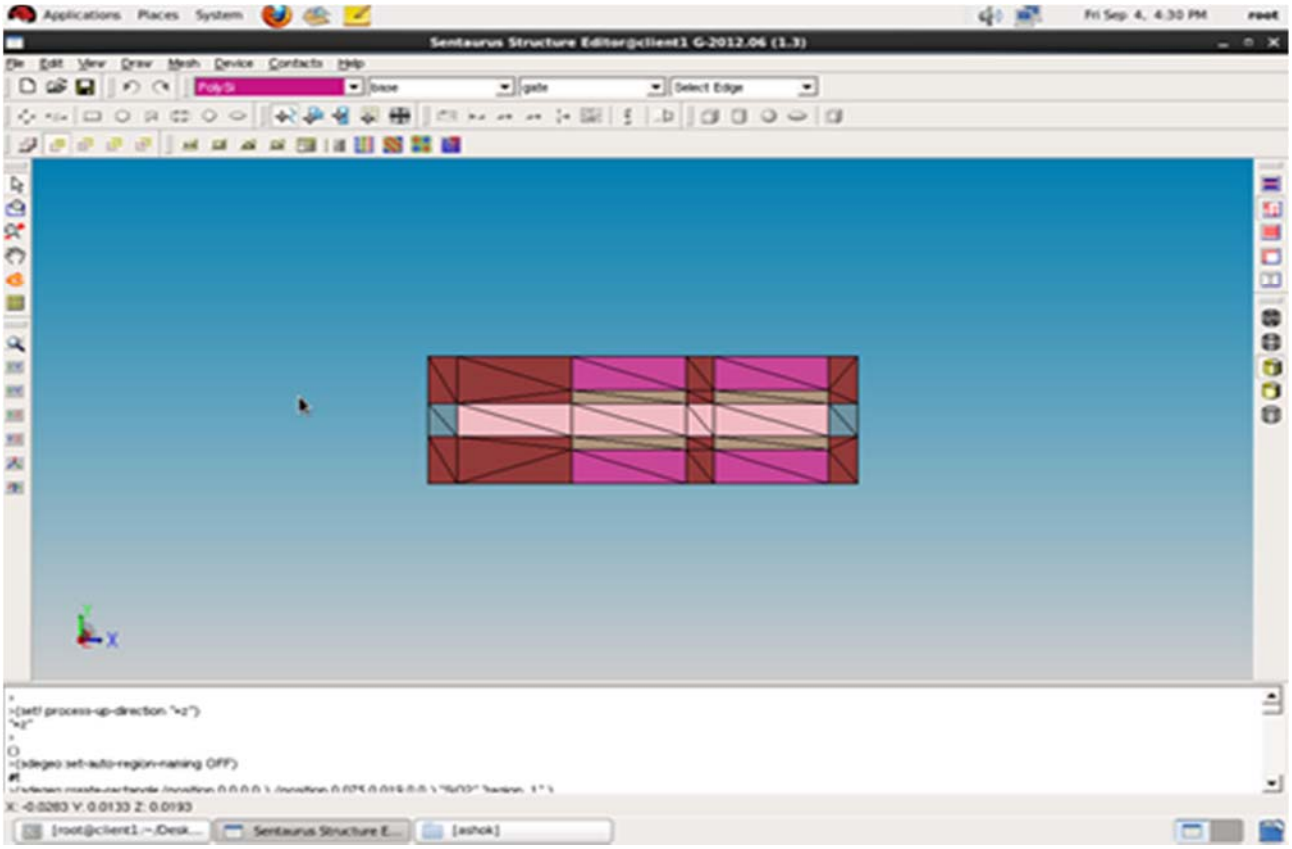
Keywords: High-k dielectric material, junction less field, effect transistor (JLFET), subthreshold slope (SS), tunnel field, effect transistor (TFET)

Introduction

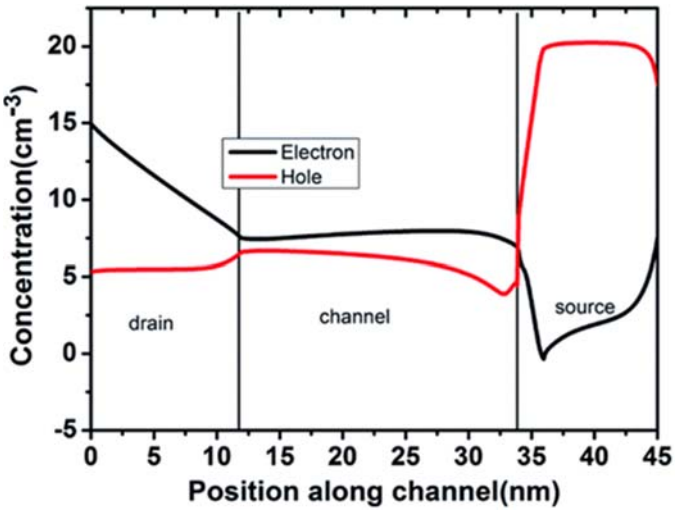
The junction field effect transistor or JFET is one of the simplest transistors from the structural point of view. It is a voltage controlled semiconductor device. In this, the current is carried by only one type of carriers. So, it is a unipolar device. It has a very high input electrical resistance. TFETs are not limited by the thermal Maxwell–Boltzmann tail of carriers, which limits the subthreshold swing of MOSFETs to 60 mV/dec at room temperature (exactly 63mV/dec. at 300K. Current swings below the MOSFET's 60-mV-per-decade limit were possible. In 2004, they reported they had created a tunnel transistor with a carbon nanotube channel and a subthreshold swing of just 40 mV per decade. JFET consists of a doped Si or GaAs bar. There are ohmic contacts, the two ends of the bar and semiconductor junction on its two sides. If the semiconductor bar is n - type, the two sides of the bar is heavily doped with p-type impurities and this is known as n - channel JFET. On the other hand if the semiconductor bar is p- type, the two sides of the bar is heavily doped with n- type impurities and this is known as p- channel JFET. When a voltage is applied between the two ends, a current which is carried by the majority carriers of the bar flows along the length of the bar.



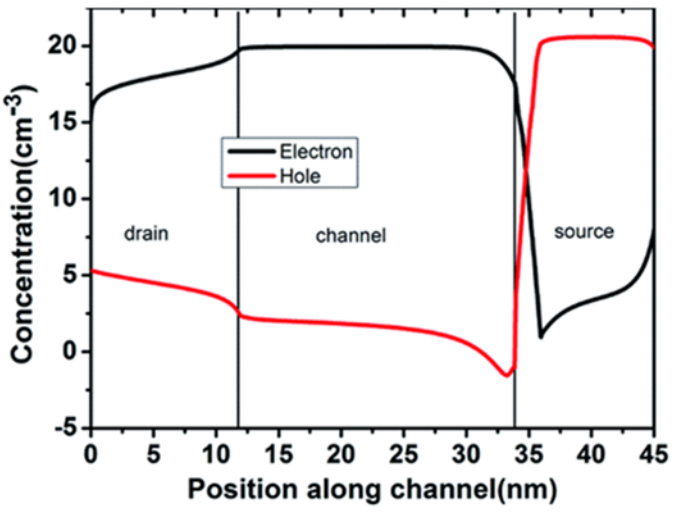
2. Device Structure & Operation: The proposed double-gate junctionless tunnel field effect transistor (JL-TFET) structure along with the lengths and thicknesses of different layers used in simulation.



The simulated JL-TFET is a Si-channel heavily n-type-doped (1×1019cm-3) JLFET with a 20-nm channel length, source/drain extension length of 20 nm, silicon film thickness of 5 nm, 2-nm gate oxide thickness, and 5 nm of isolation in between Control-Gate (CG) and P-Gate (PG), which works as an isolation between the gates and also as a spacer. The double-gate technology is used to provide better controllability over the channel. All simulations are carried out using a 2-D device simulator.



A nonlocal band-to-band tunneling (BTBT) model is used, and this model has been used in the literature to predict the performance of TFET. The nonlocal BTBT model is used in the simulation to take into account a tunneling along the lateral direction. Band-gap narrowing (BGN) model is also enabled due to high doping concentration in the channel. The gate leakage current model is not included, with the assumption of high-k metal gate stack. Shockley-Read-Hall (SRH) recombination model is also included because of a presence of high impurity atom in the channel and also consideration of an interface trap (or defect) effect. The quantum confinement effect and interface trap effect on BTBT in TFETs are also enabled, by inclusion of quantum confinement (QC) model, and trap-assisted tunneling (TAT) model. The following sorting mechanisms can be adopted for the database management and supporting the feedback loop.



3. Results & Discussions

the electron and hole concentration profile in the OFF state, from the concentration profile it is observed that the device looks like an N+-I-P+-doped device structure. The OFF-state energy-band diagram is shown. In this case, the probability of the tunneling of electrons is negligible, since the tunneling barrier in between the source and channel is very large, so the OFF-state current flows only because of an N+-I-P+ diode leakage. The device is turned on, by applying a gate voltage on the Control-Gate, which narrows the barrier between the source and channel of the device. The ON-state electron and hole concentration profile is shown. From the figure, we observe that on applying a gate voltage on the Control-Gate, the electron concentration of the device layer beneath this gate increases and becomes almost an n-type region. This results in narrowing of the barrier between the source and channel of the device. For a TFET, it is found that the ON current (ION) increases exponentially with decrease in the tunneling barrier width. Shows the ON-state energy band diagram, in which we observe that the tunneling barrier between source and channel of the device has lowered significantly, so there is a high probability of tunneling of electrons from a valence band of the source to the conduction band of the channel. Hence, significant amount of current flows because of the quantum tunneling mechanism. Like in a TFET, we apply gate voltage only on the Control-Gate (the gate above the intrinsic region of the device) to turn on the device. The voltage of Control- Gate (CG) is varied from 0 to 1 V for turning the device ON.

Either in an OFF state or ON state, P-Gate terminal is kept at zero bias. It has been shown that the use of high-k dielectric gate material for TFETs improves the ON current and also SS. Although the use of high-k dielectrics gives advantages in device characteristics, however, when high-k dielectric material is directly put in contact with silicon channel, it can lead to defects at the dielectric/semiconductor interface. The effect of interface defects is also taken into consideration for the simulation of TFETs. Here in the proposed structure, we have considered different dielectric materials (such as TiO2 ($\varepsilon r = 80$), La2O3 ($\varepsilon r = 30$), HfO2 ($\varepsilon r = 25$), Al2O3 ($\varepsilon r = 9$), Si3N4 ($\varepsilon r = 7$), SiO2 ($\varepsilon r = 3.9$)), and the dielectric constants of different materials are taken from. The subthreshold characteristic of the proposed device with high-k dielectric materials is shown in Fig. 4(a); here the QC model is not included. It is clear from figure that the material with higher dielectric constant gives a higher ON current and also improved SS. The improved ION and SS are observed, because of a higher gate coupling offered by high-k dielectric gate material of higher dielectric constant value ranging from 3.9 to 80, keeping the physical thickness of gate oxide fixed and equal to 2nm. The point SS is measured as the inverse of maximum slope of the log of the drain current versus gate voltage. The average SS is measured as used. The ON current (ION) and OFF current (IOFF) are measured at the supply voltages of (VDS = 1V, VCGS = 1 V) and (VDS = 1V, VCGS = 0V), respectively. The highest ON current of ~ 36μ A/μm is achieved for a high-k dielectric material of TiO2. Very low OFF current (<~5×10-14 A/μm) is also observed for all considered high-k dielectric materials.

4. Conclusion

In this research paper, i proposed and discussed the basic static operation of JL-TFET in which there is no p–n junction and which gives the combined advantages of conventional TFET and JLFET. The high-k dielectric gate material for JL-TFETs is used to improve the ON current and SS. The proposed device structure exhibits excellent ON–OFF characteristics based on our simulations. It seems to be a very promising device for sub-22-nm nodes.

5. Acknowledgment

I wish to thank my mentors and college for supporting us in completing our work on Machine Learning Algorithm Hypothesis on Smart Gyroscopic Tuned Dampers for Earthquake Resistance Buildings. I also wish to thank my parents for providing us with assets that helped us completing research regarding this concept.

6. References

1. DeMicheli G, Leblebici Y, Gijs M, Vörös JNanosystems Design and Technology. Springer, doi: 10.1007/978-1-4419-0255-9, 2009.
2. http://dx.doi.org/10.1103/PhysRevLett.93.196805.
3. Seabaugh AC, Zhang Q. Low-Voltage Tunnel Transistors for Beyond CMOS Logic, Proceedings of the IEEE doi: 10.1109/JPROC.2010.2070470, 2010; 98(12):2095-2110.
4. The Tunneling Transistor. Seabaugh Teherani, JT, Agarwal S, Yablonovitch E, Hoyt JL, Antoniadis DA. Impact of Quantization Energy and Gate Leakage in Bilayer Tunneling Transistors. IEEE Electron Device Letters doi:10.1109/LED.2012.2229458. 2013; 34(2):298.
5. Device Simulation of Tunnel Field Effect Transistor (TFET). Huang, 2013.